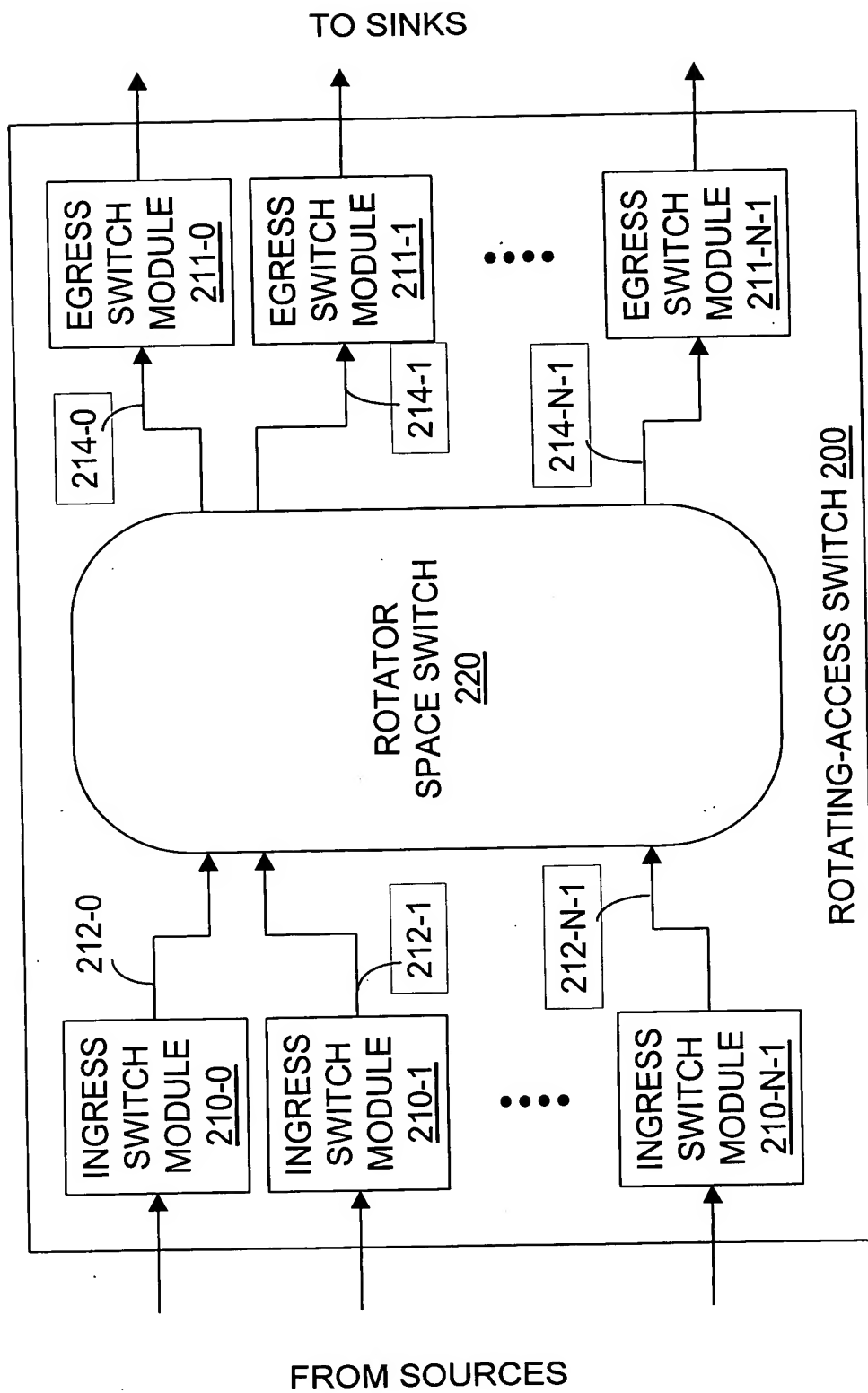


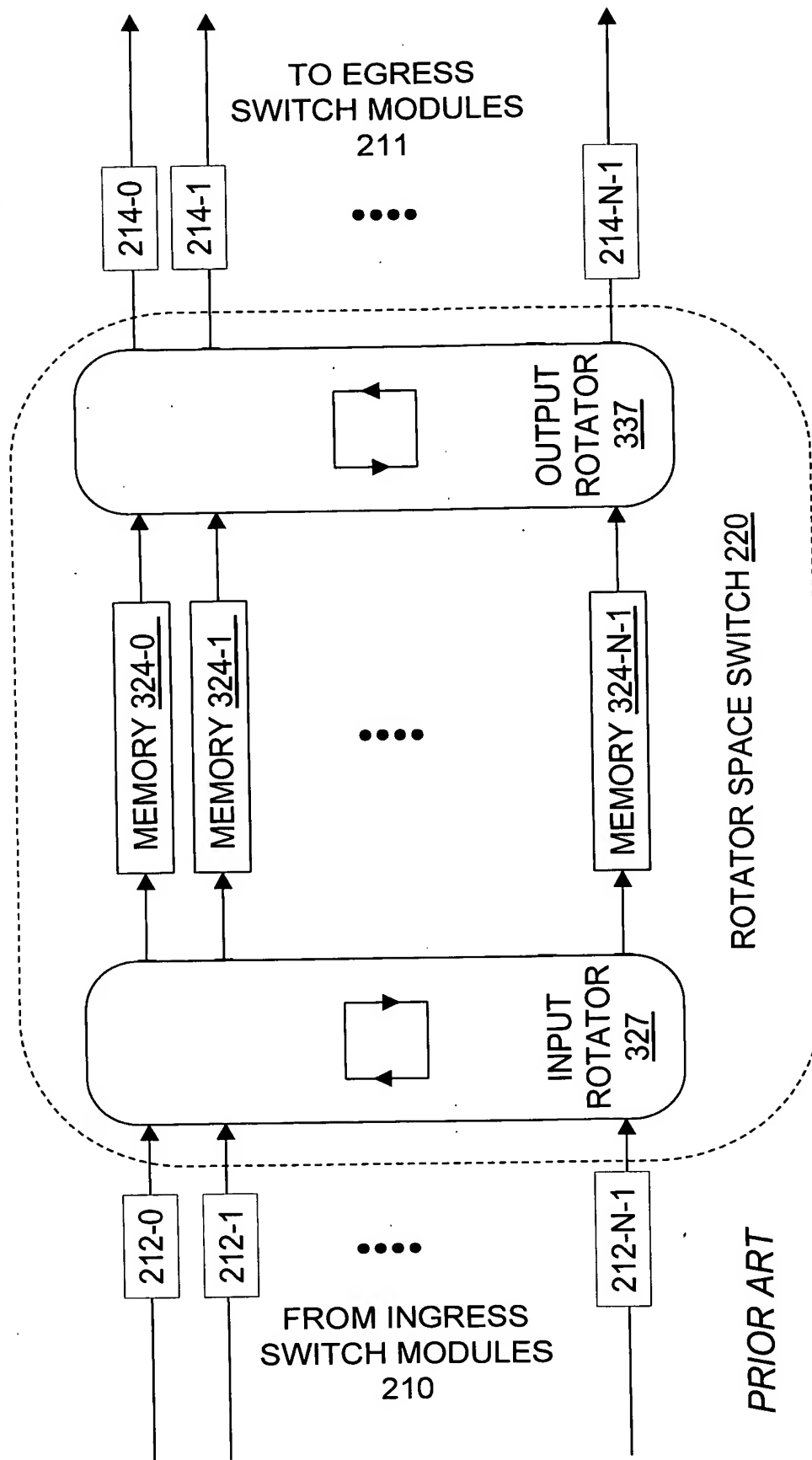
PRIOR ART

FIG. 1

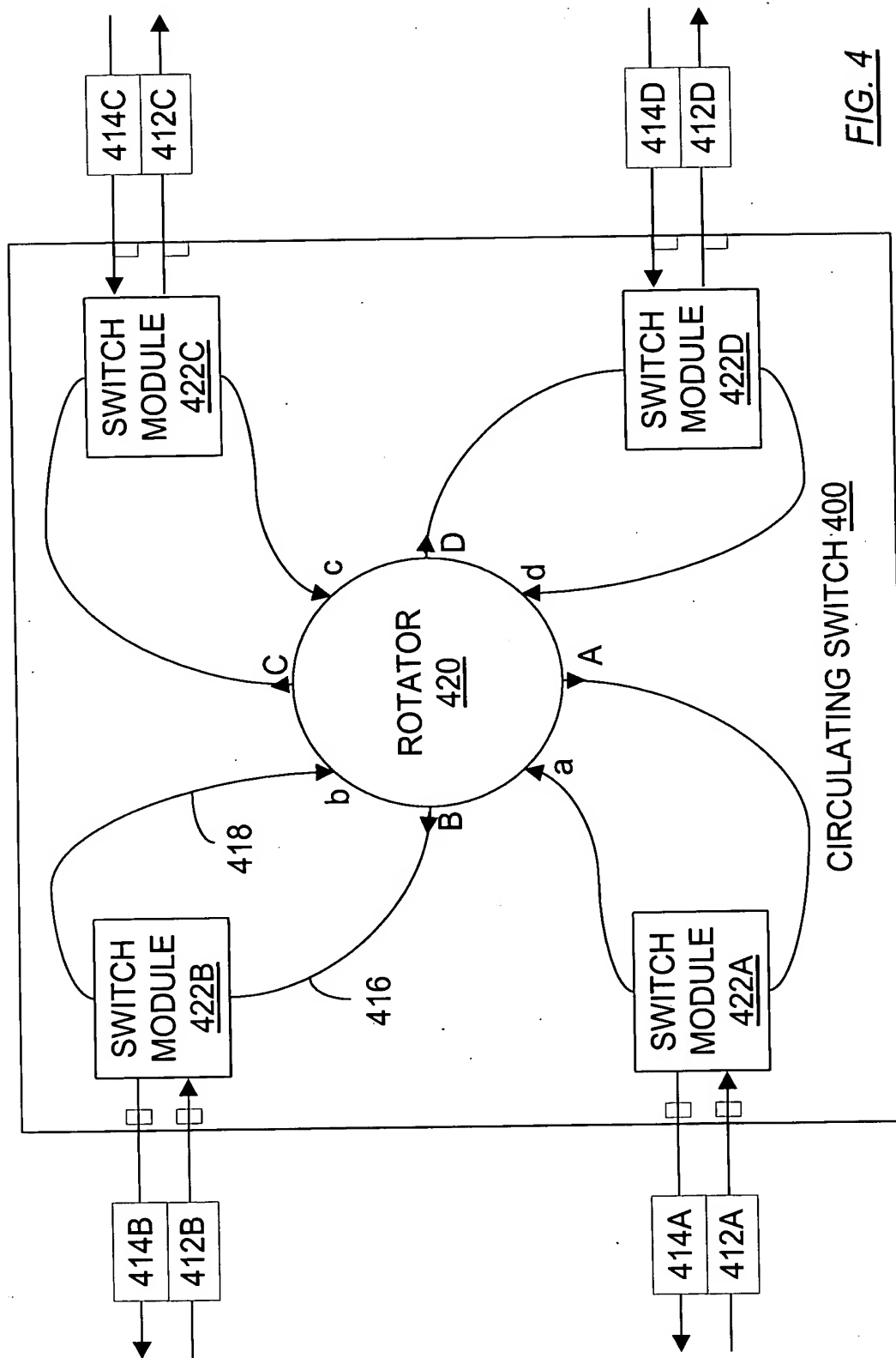


**FIG. 2**

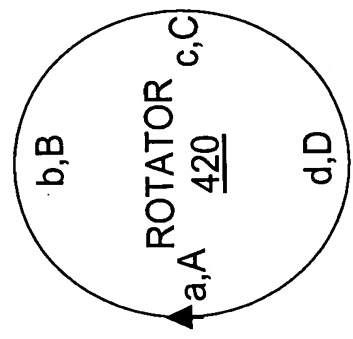
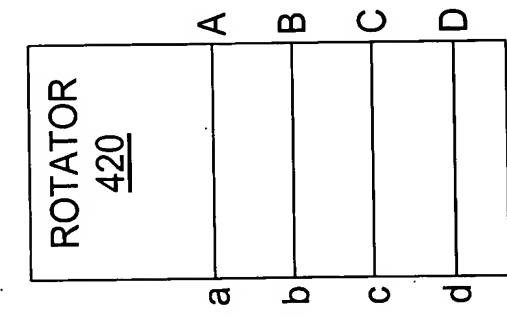
PRIOR ART



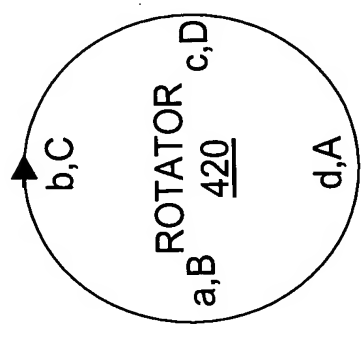
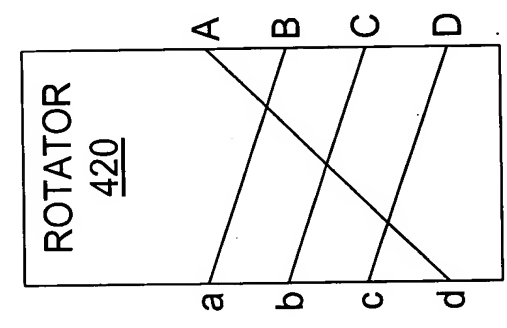
**FIG. 3**



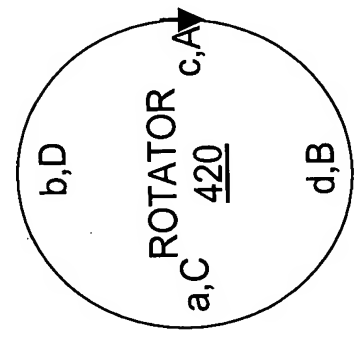
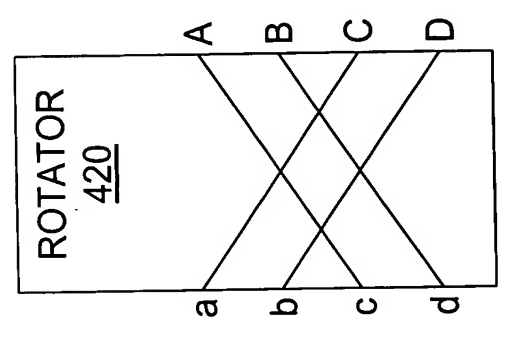
**FIG. 4**



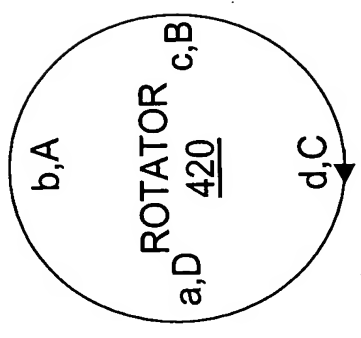
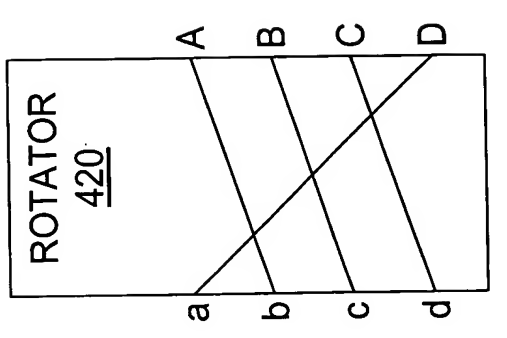
PHASE-0  
552



PHASE-1  
554



PHASE-2  
556



PHASE-3  
558

FIG. 5

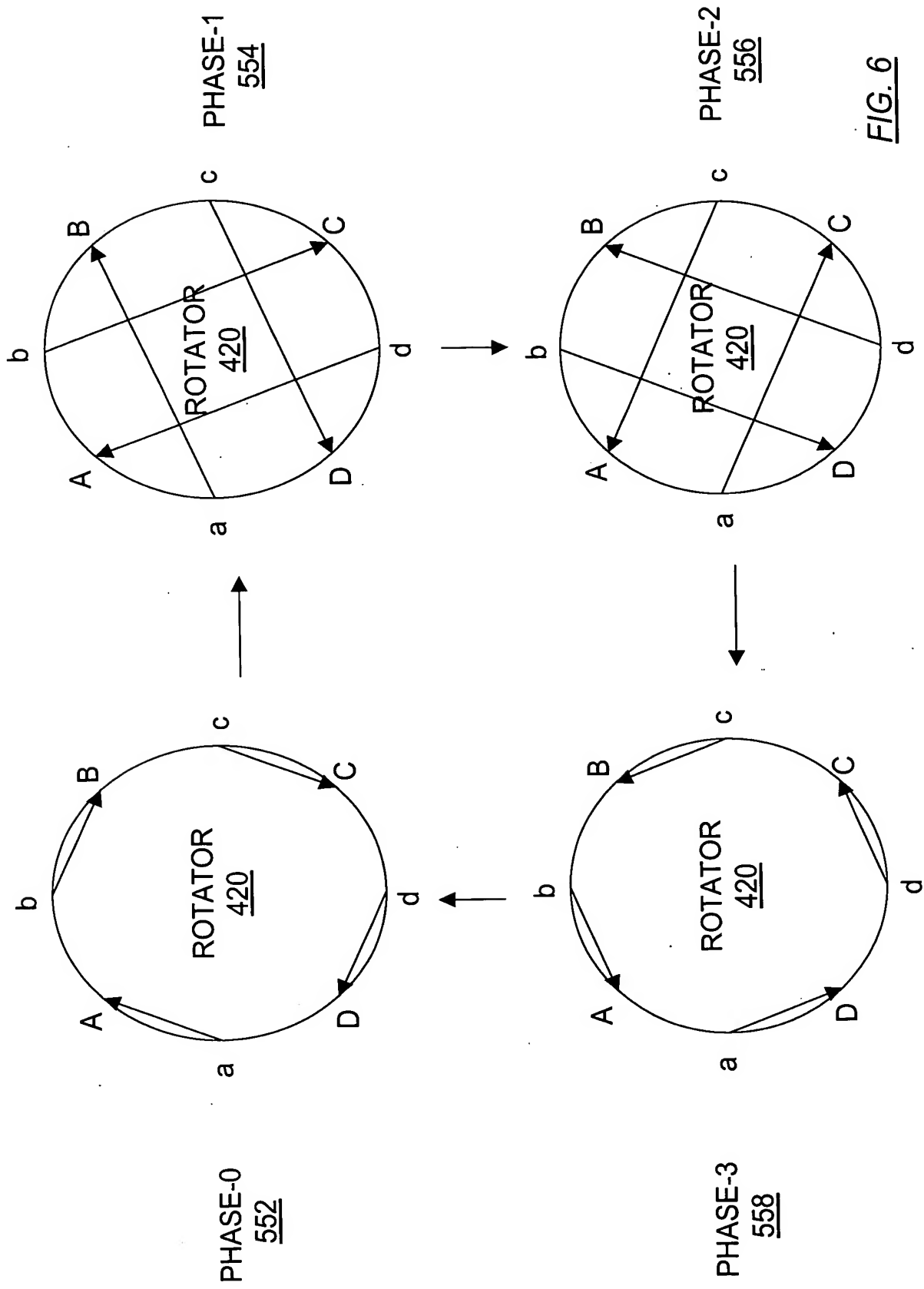


FIG. 6

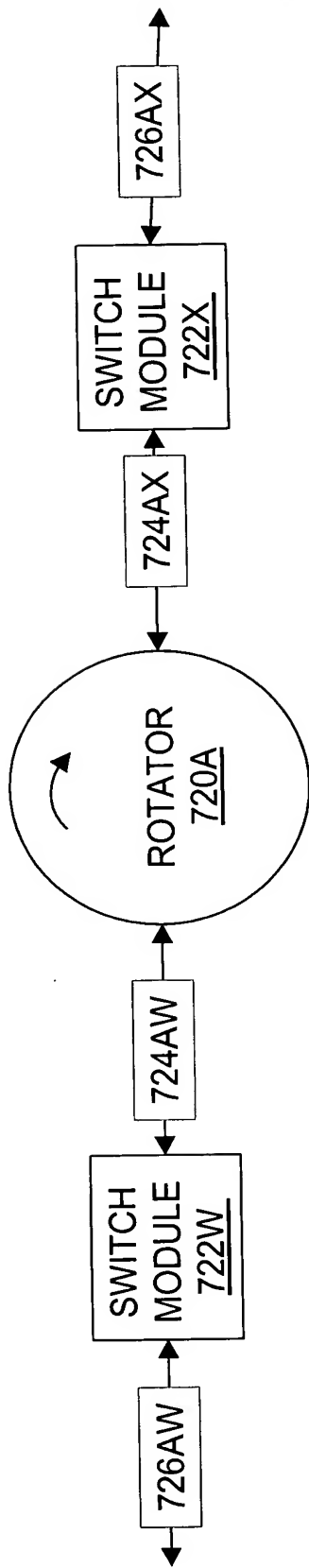


FIG. 7A

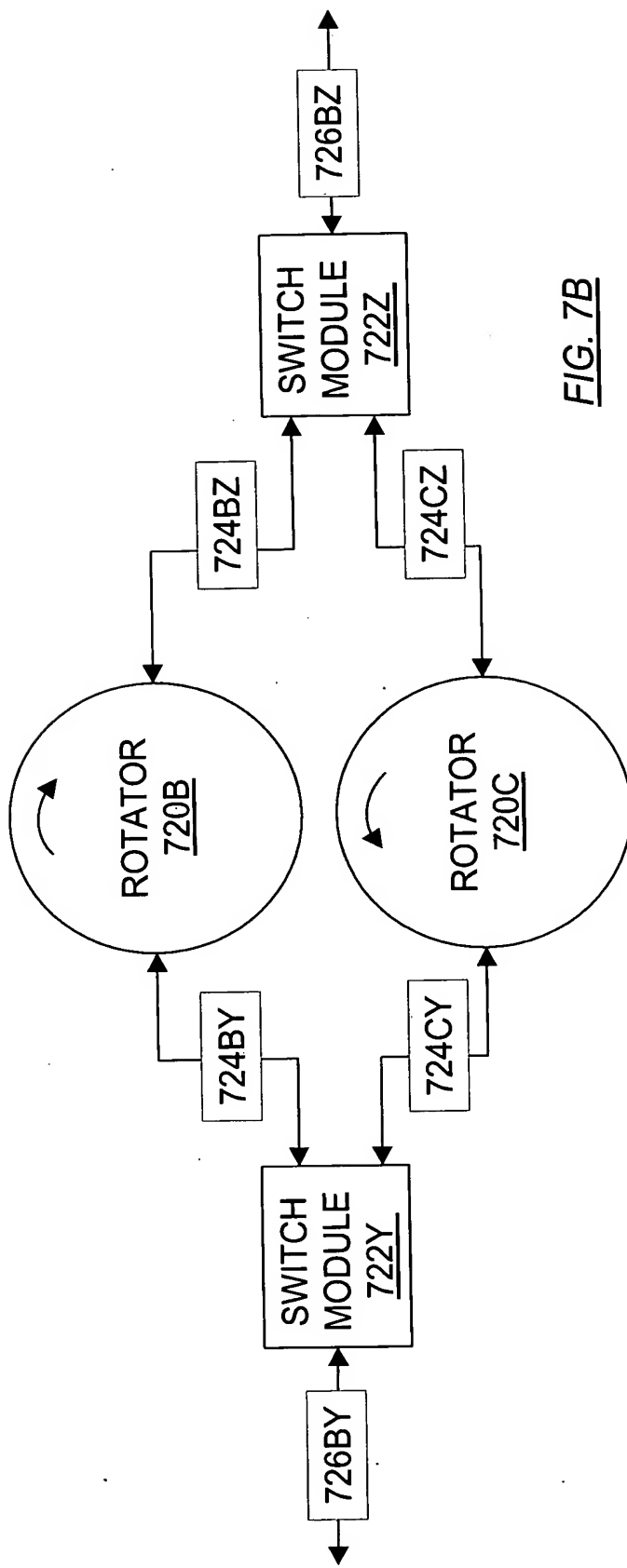
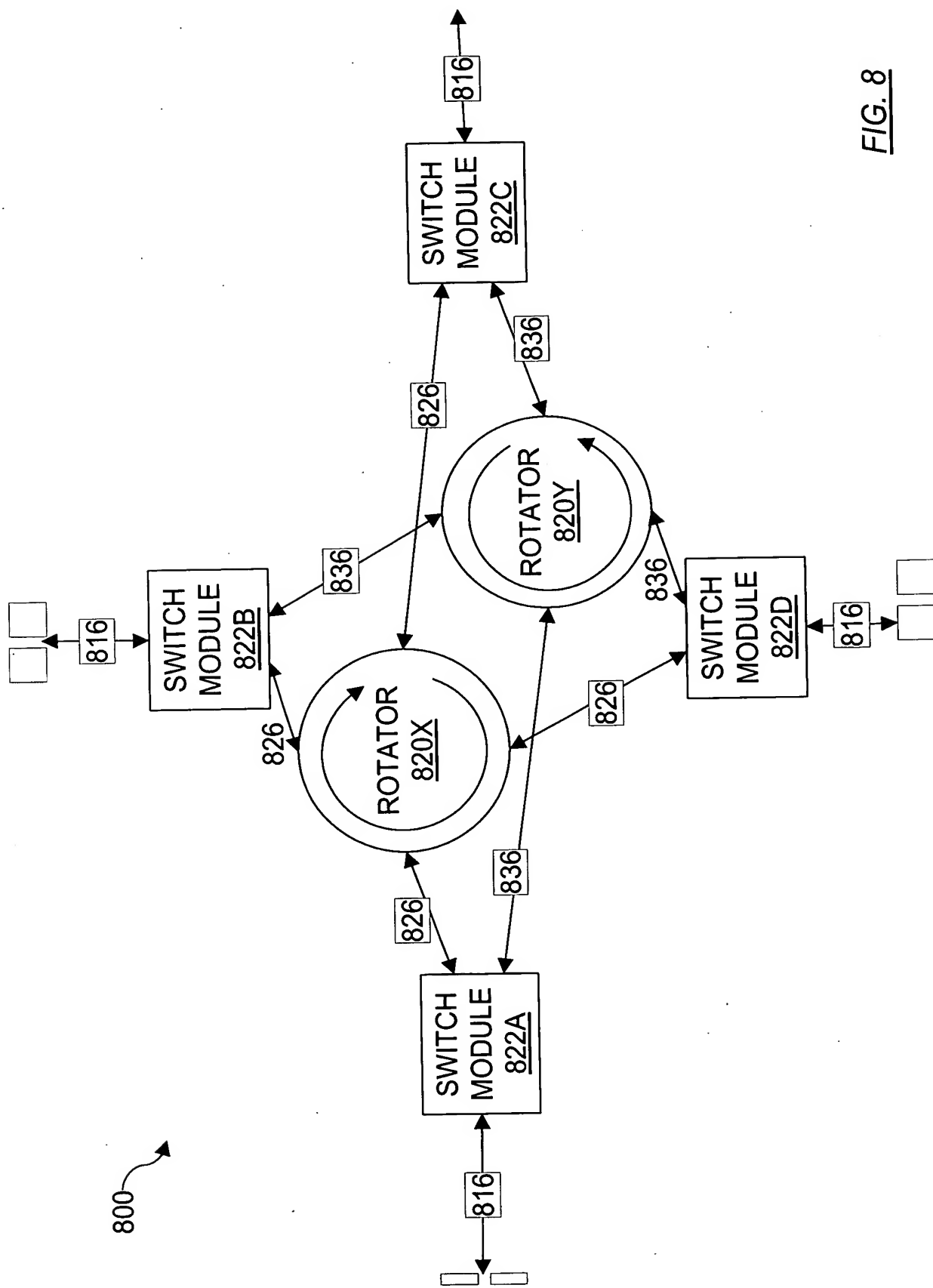


FIG. 7B



**FIG. 8**



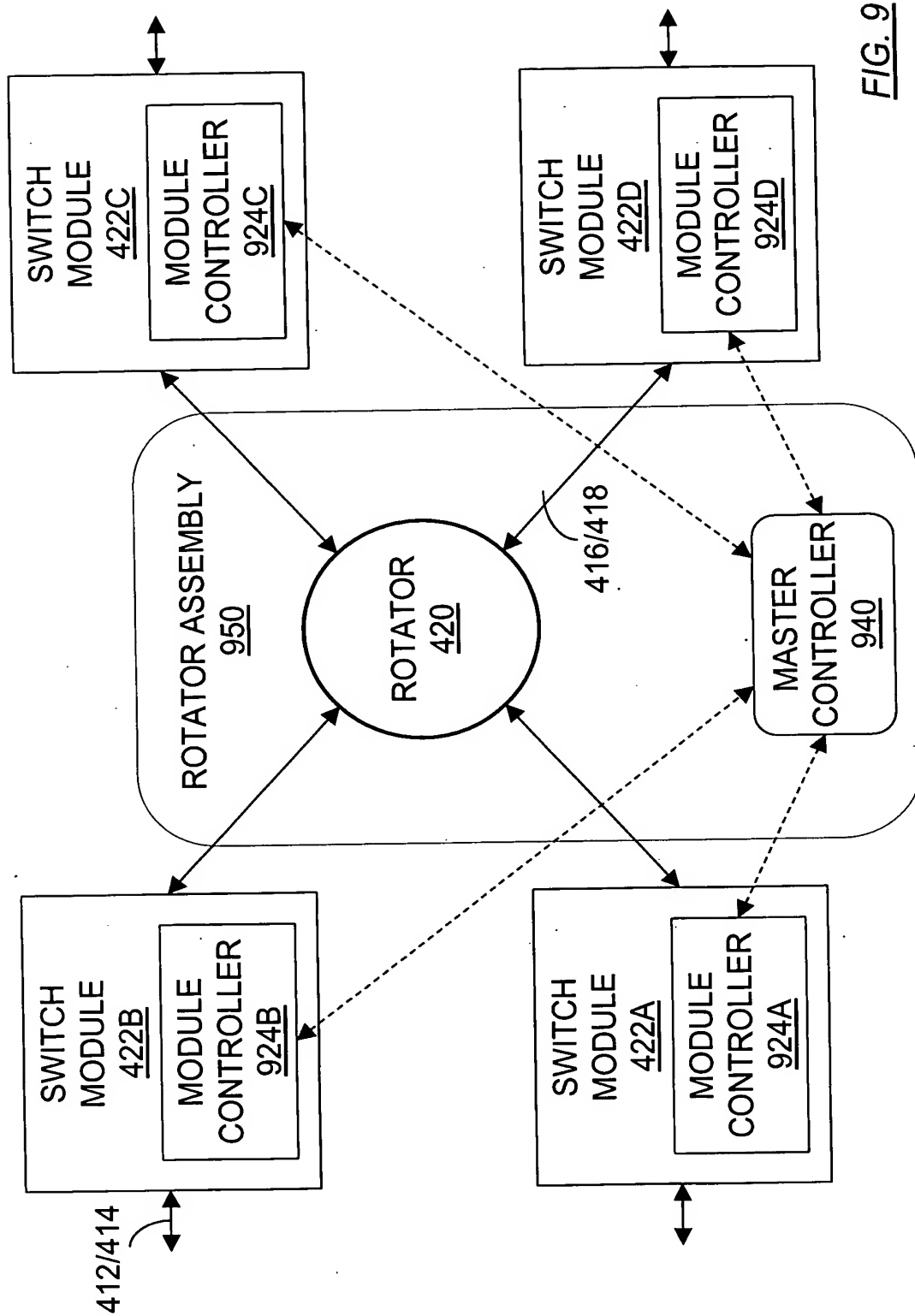


FIG. 9

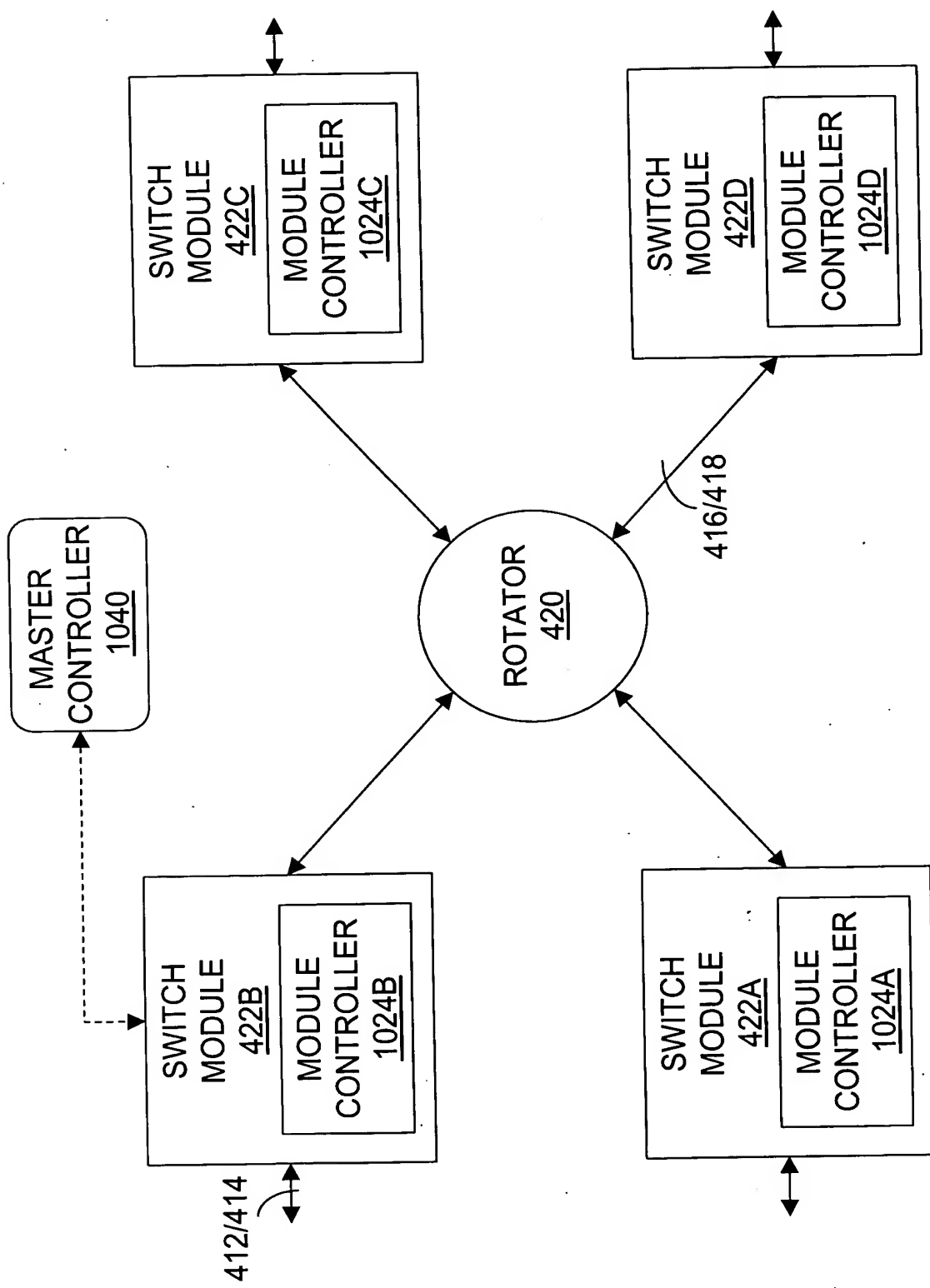


FIG. 10

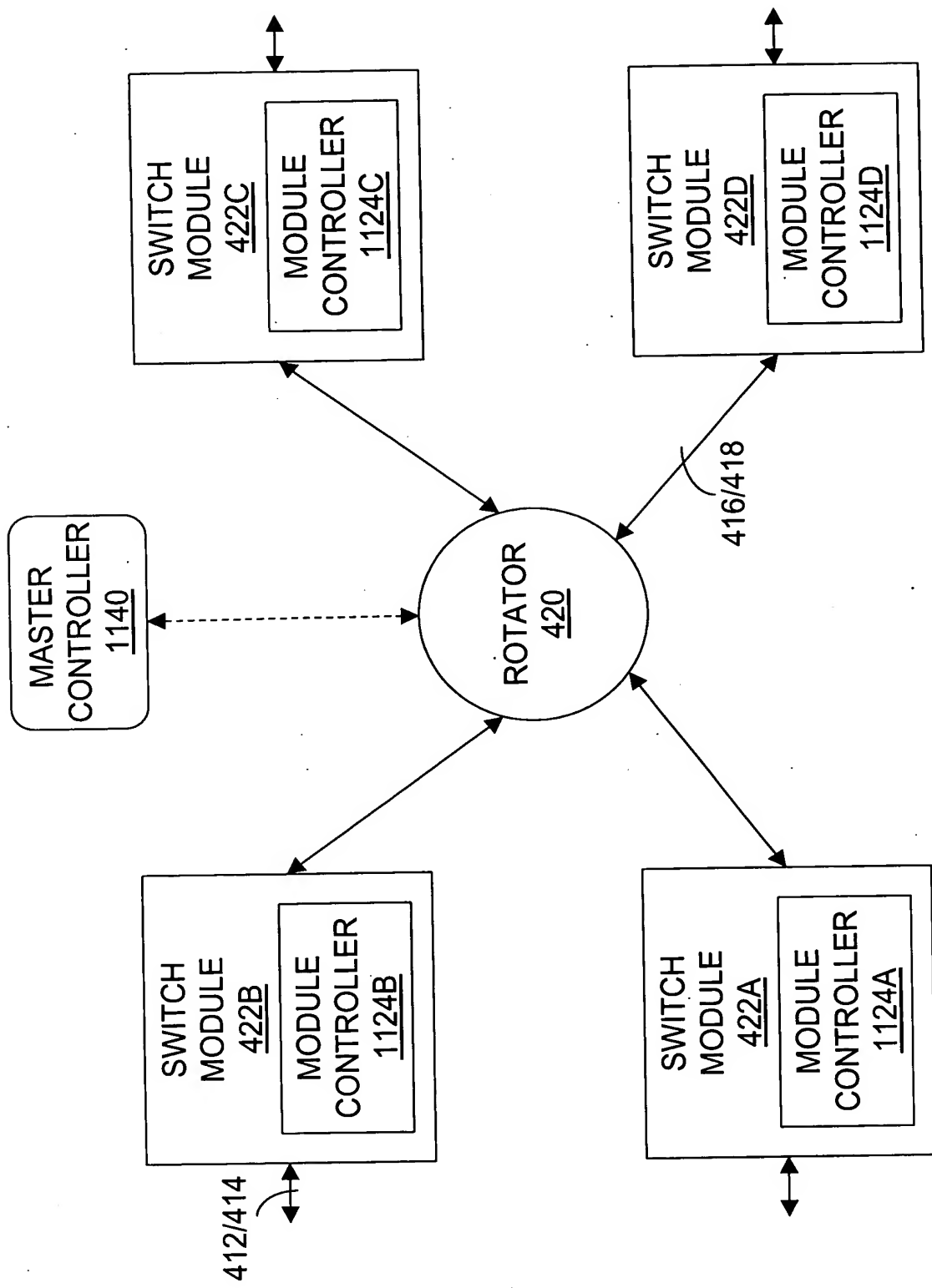


FIG. 11

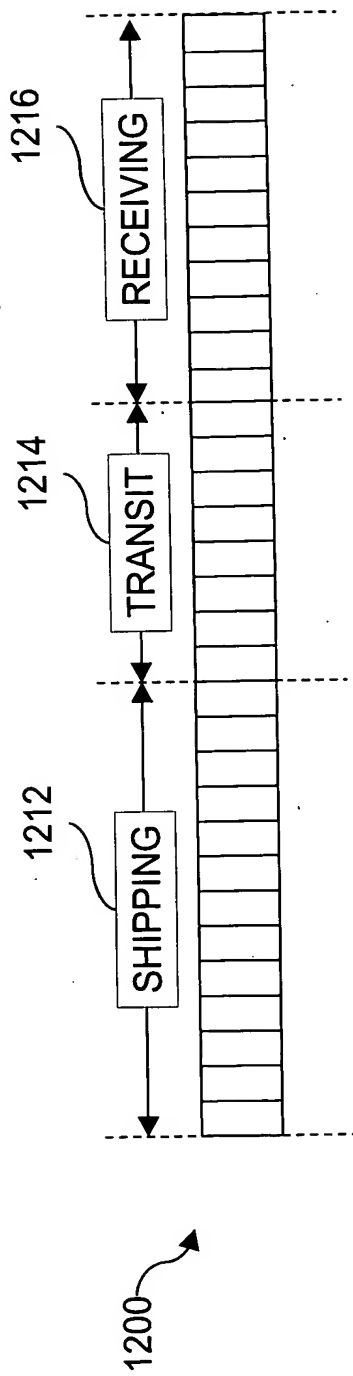


FIG. 12

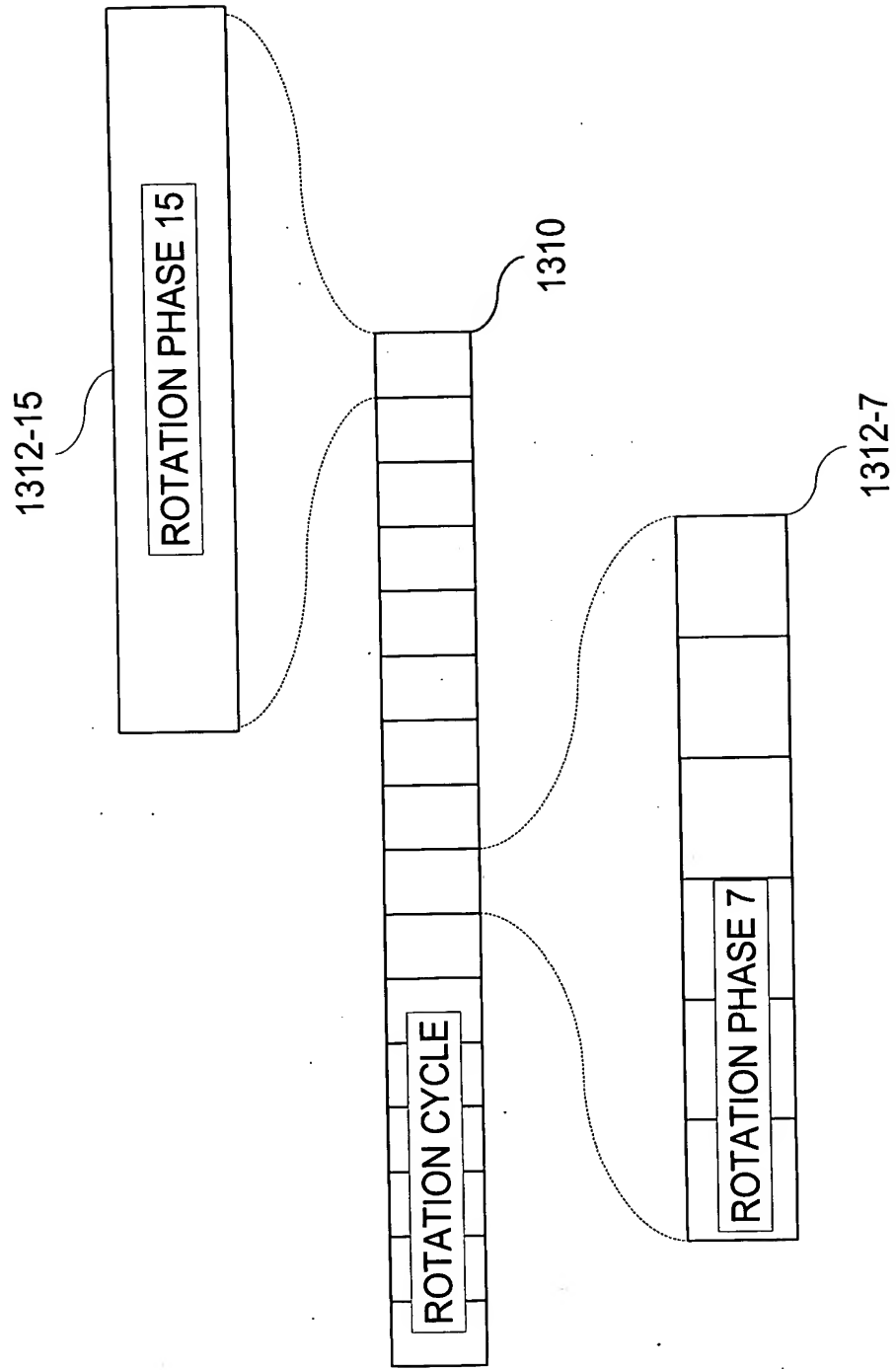


FIG. 13

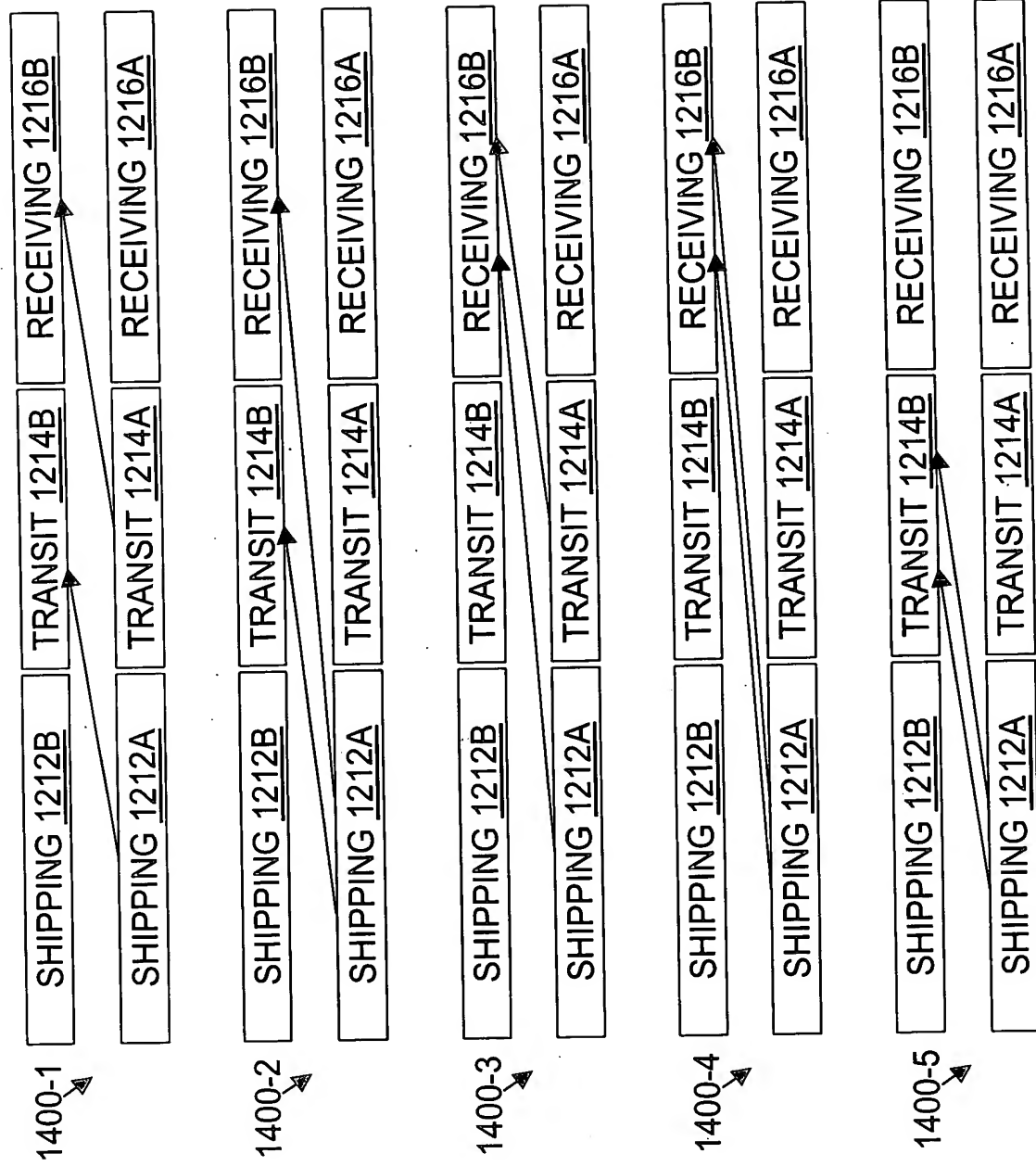
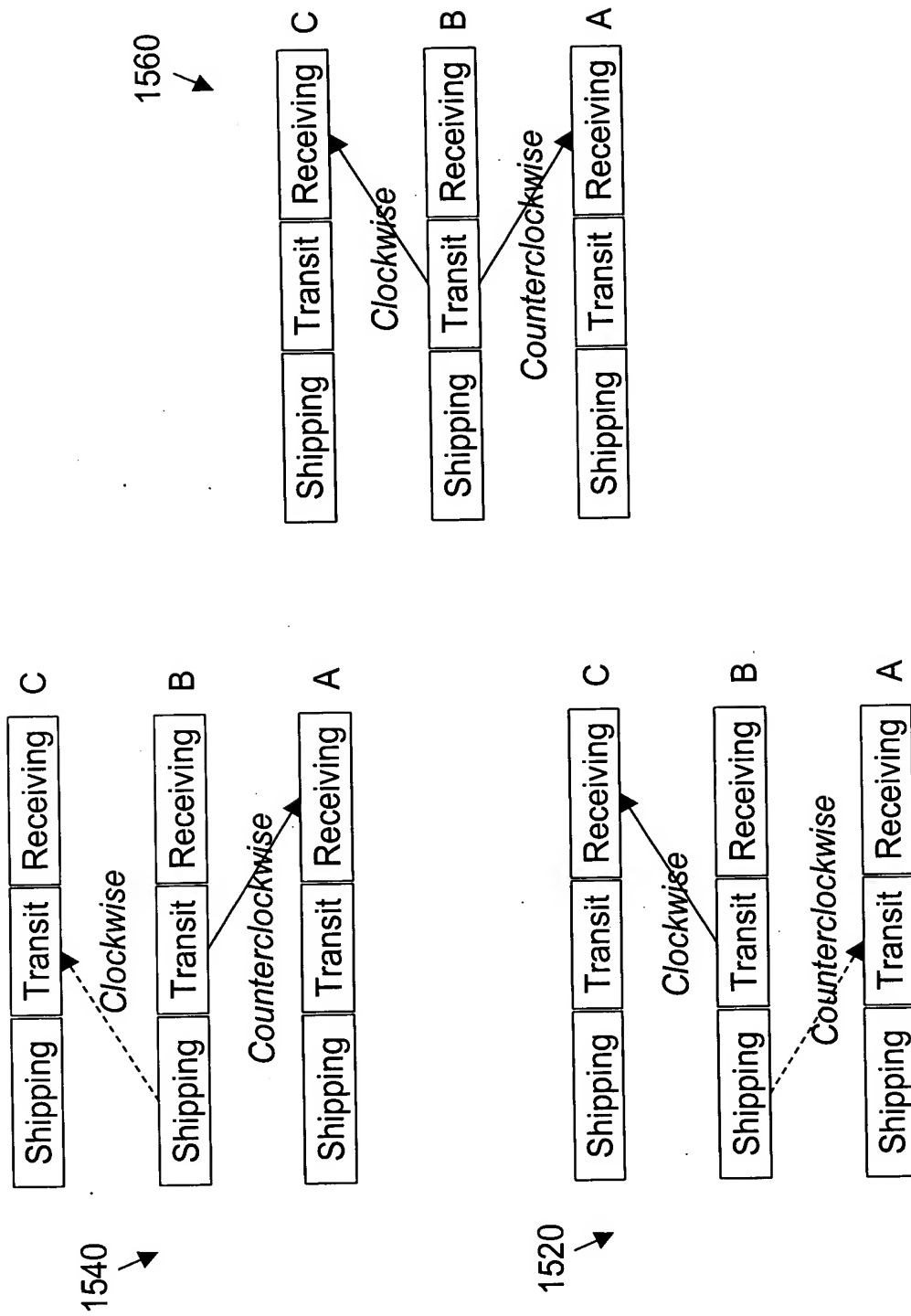


FIG. 14



**FIG. 15**

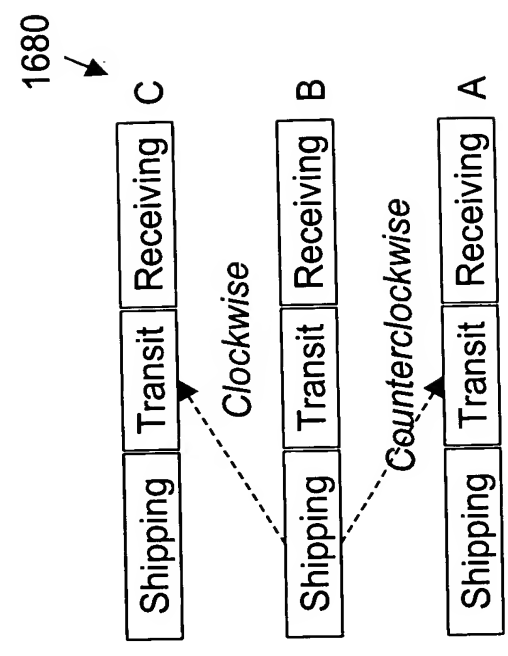
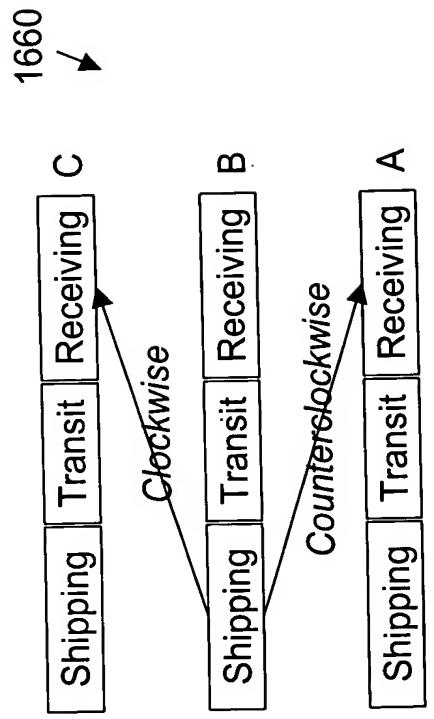
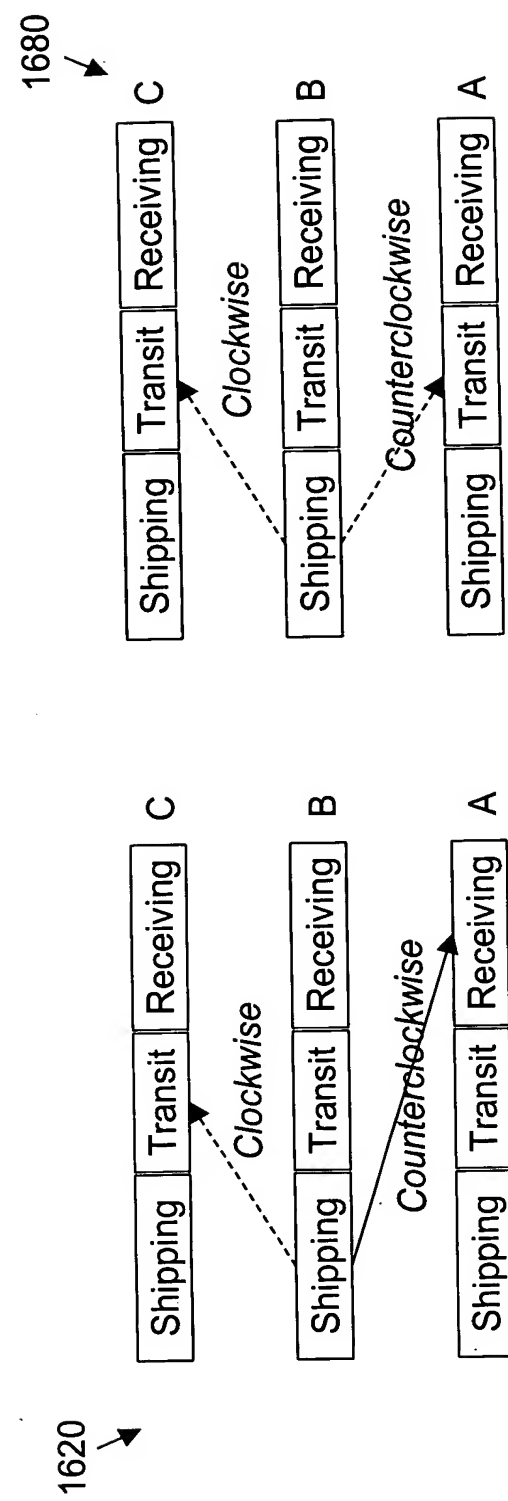
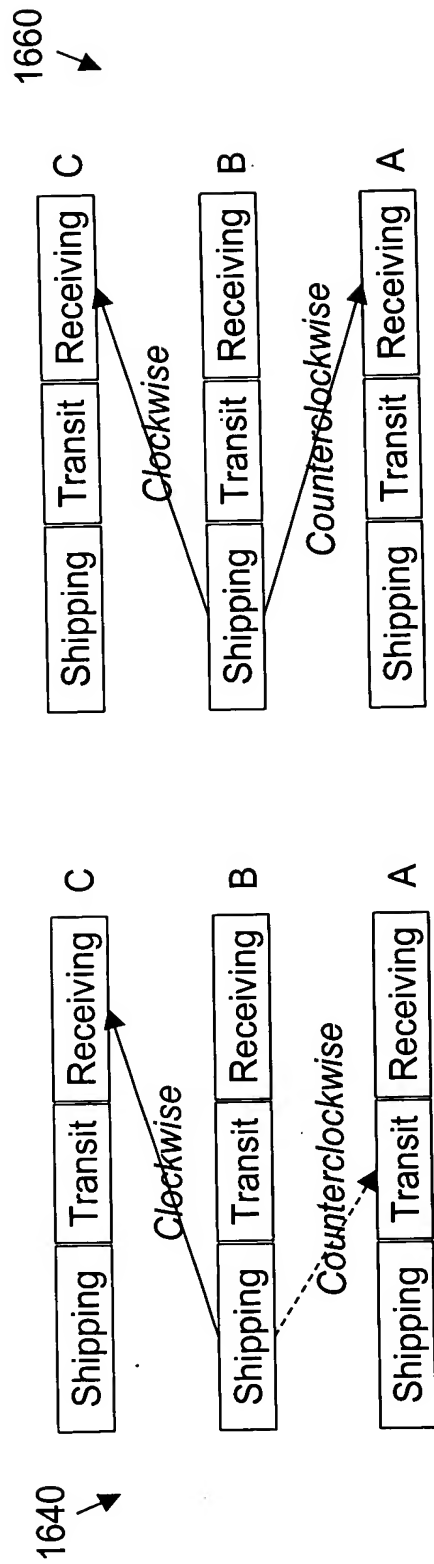
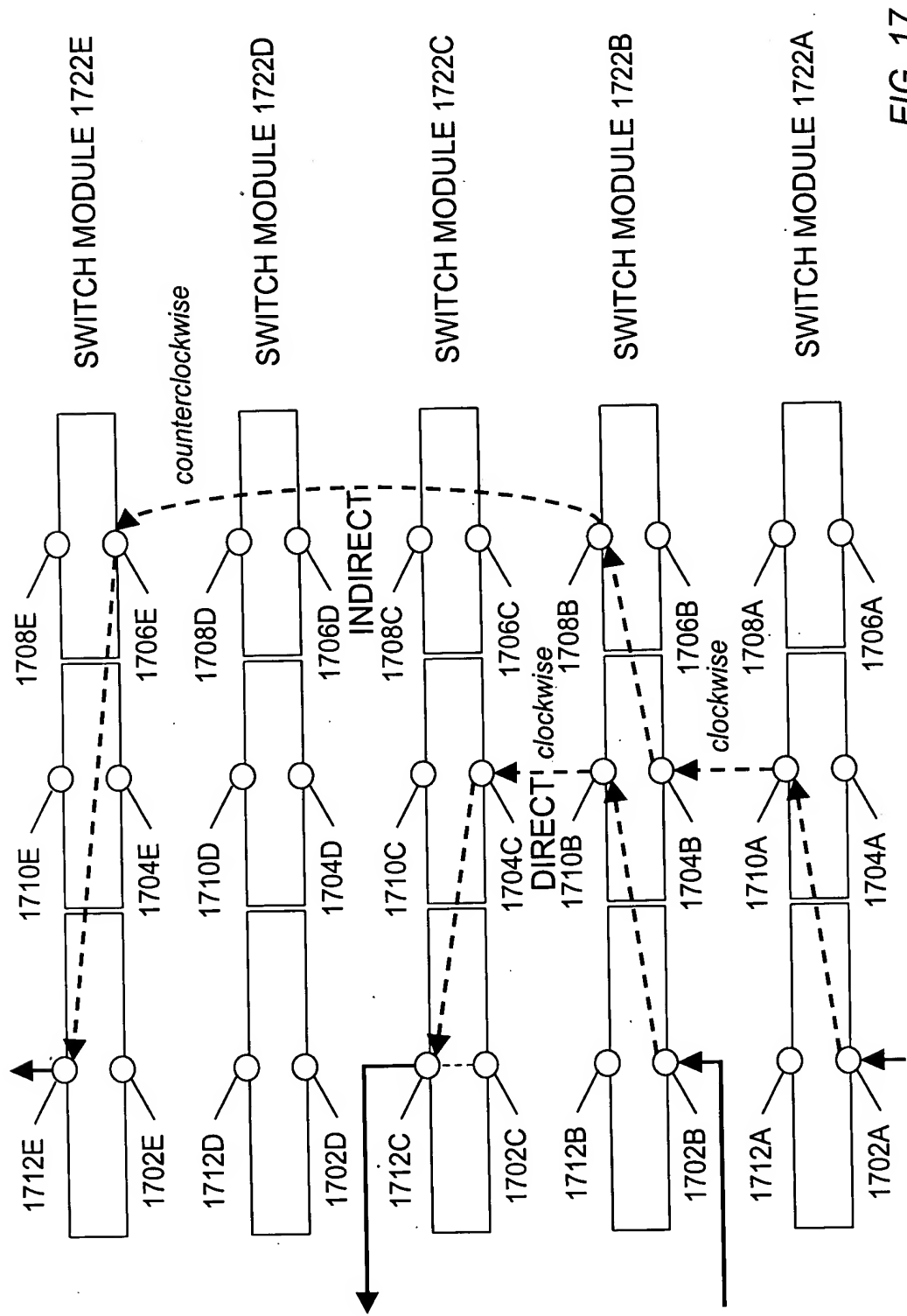
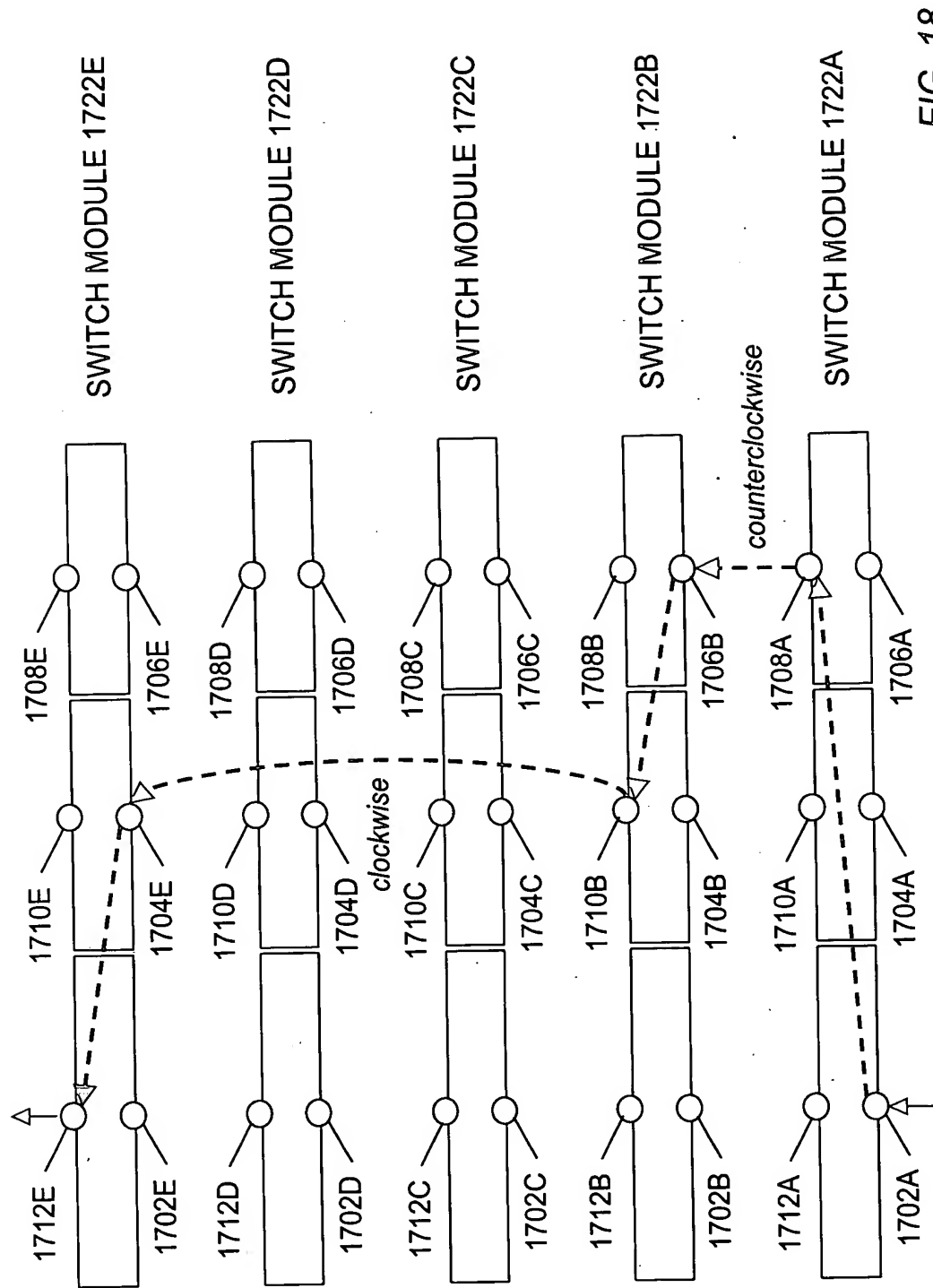


FIG. 16





**FIG. 17**



**FIG. 18**

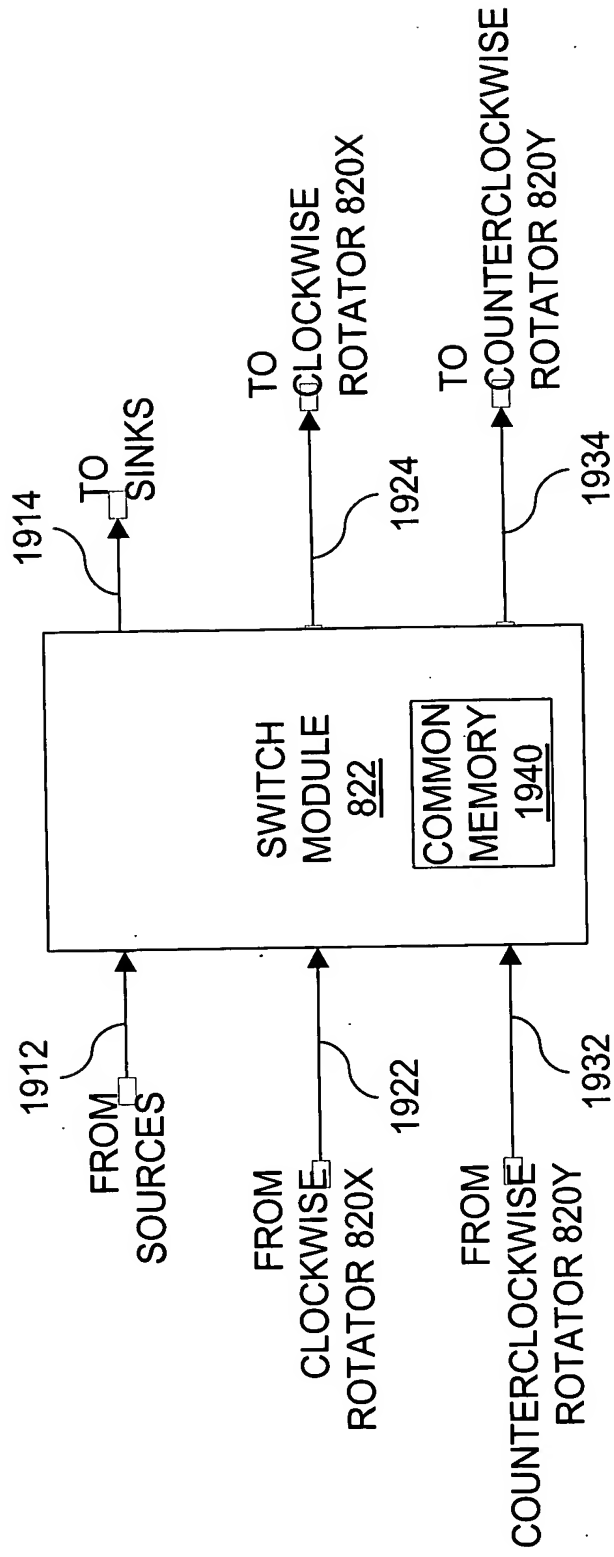


FIG. 19

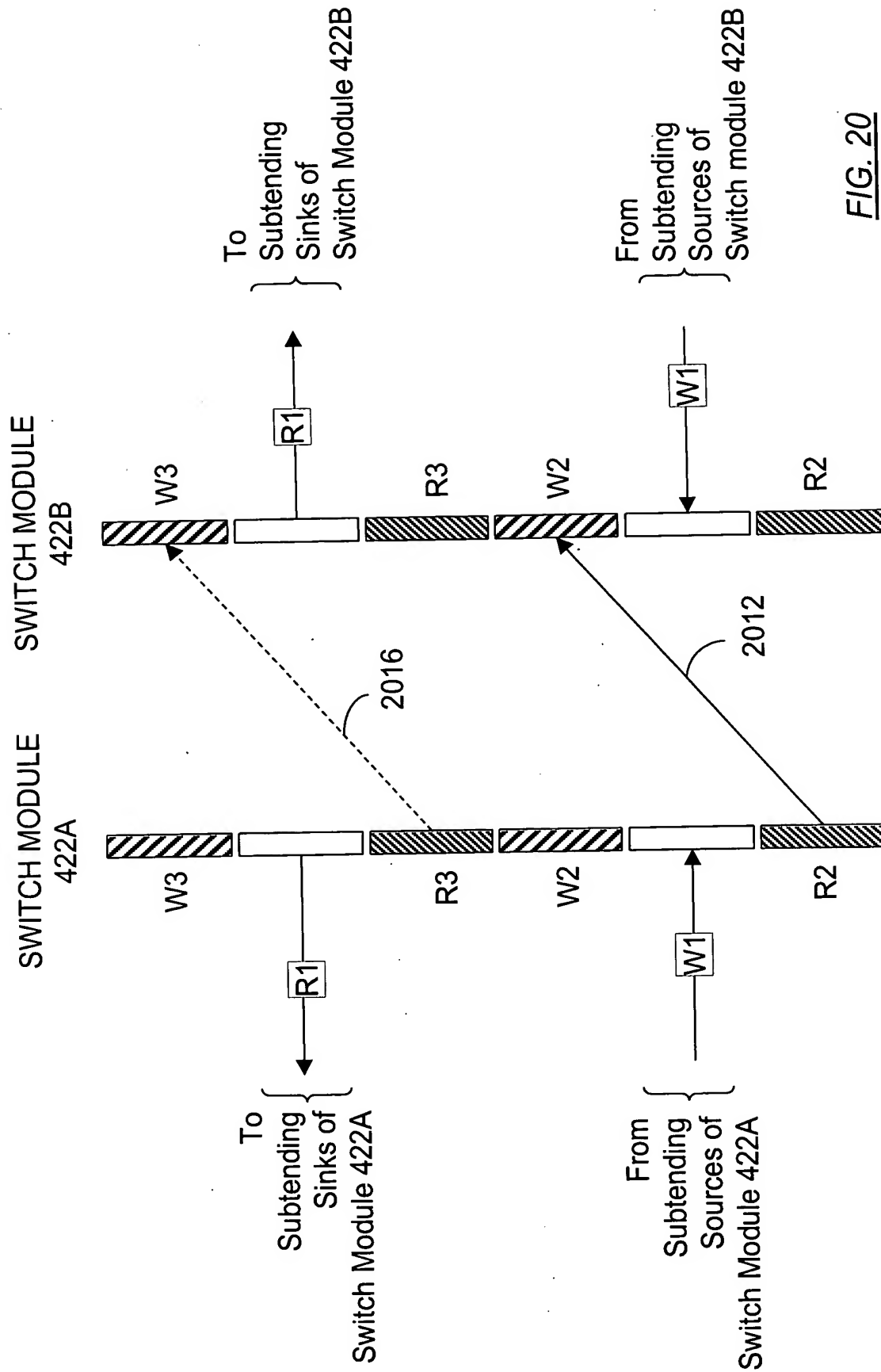


FIG. 20

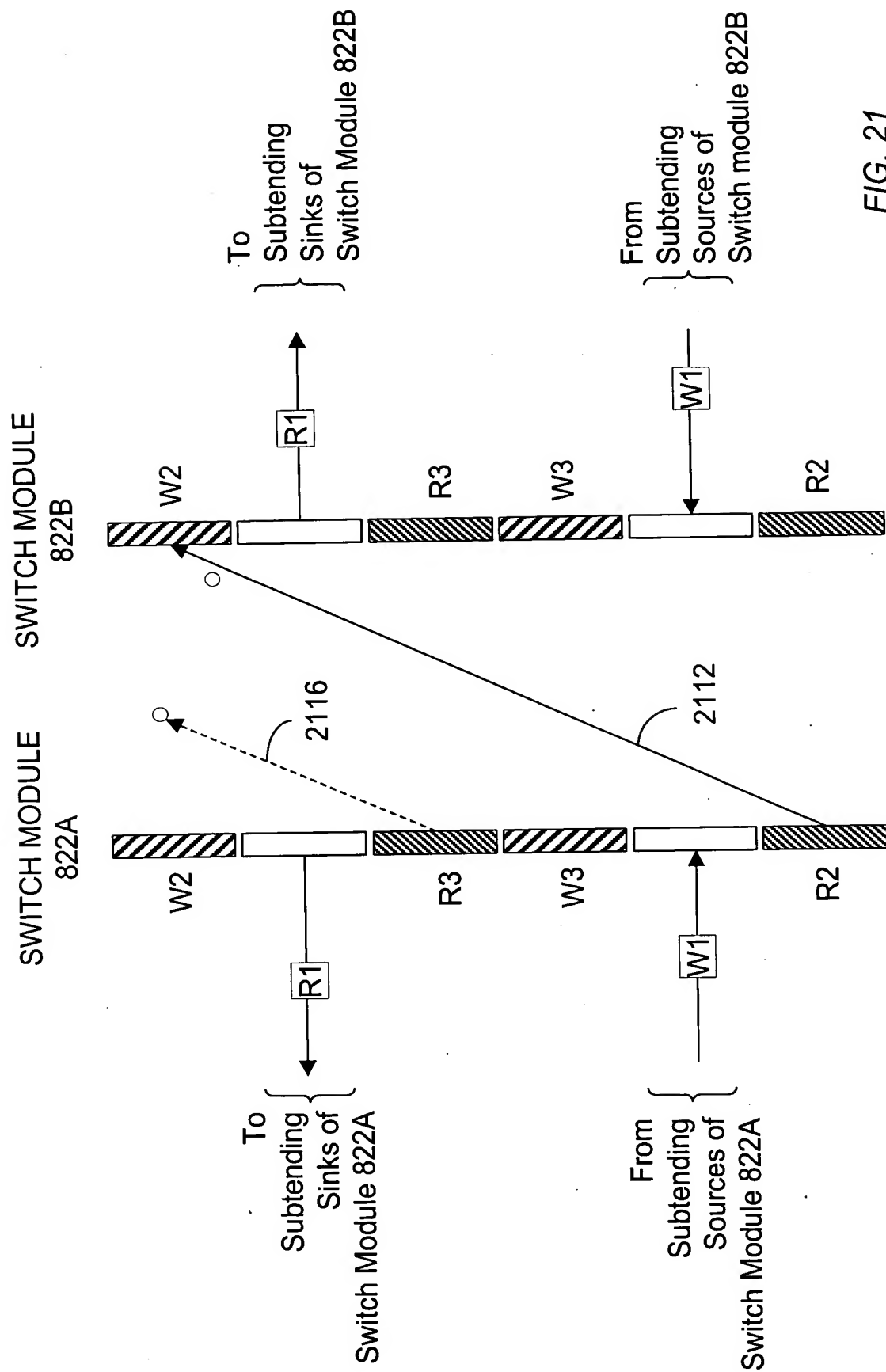
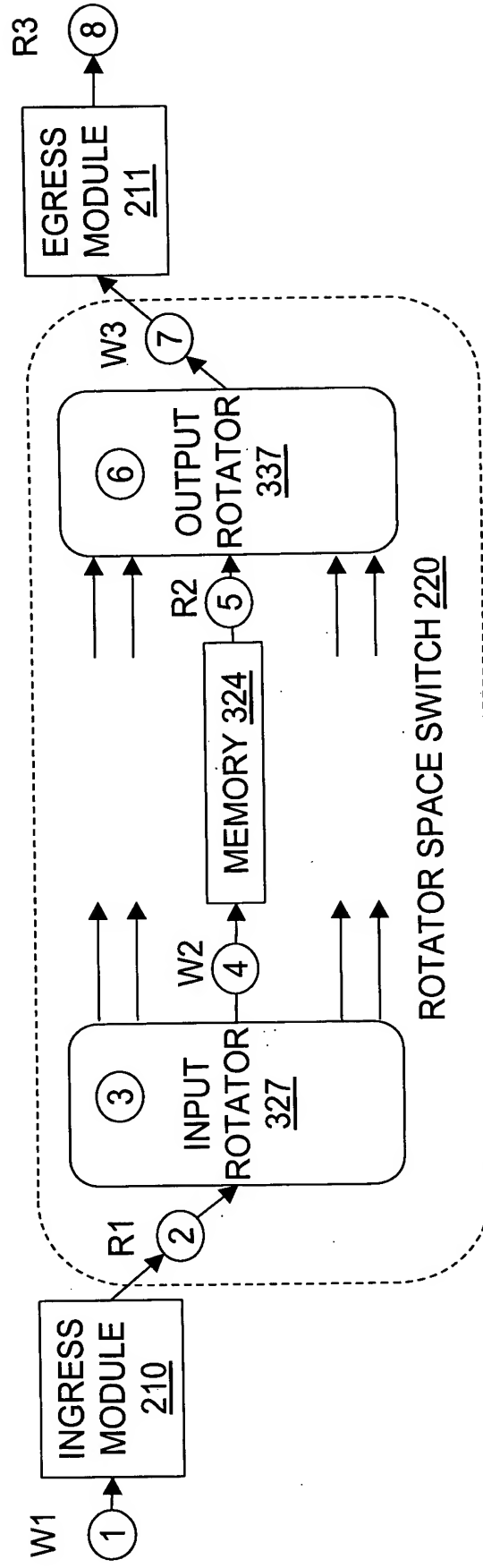
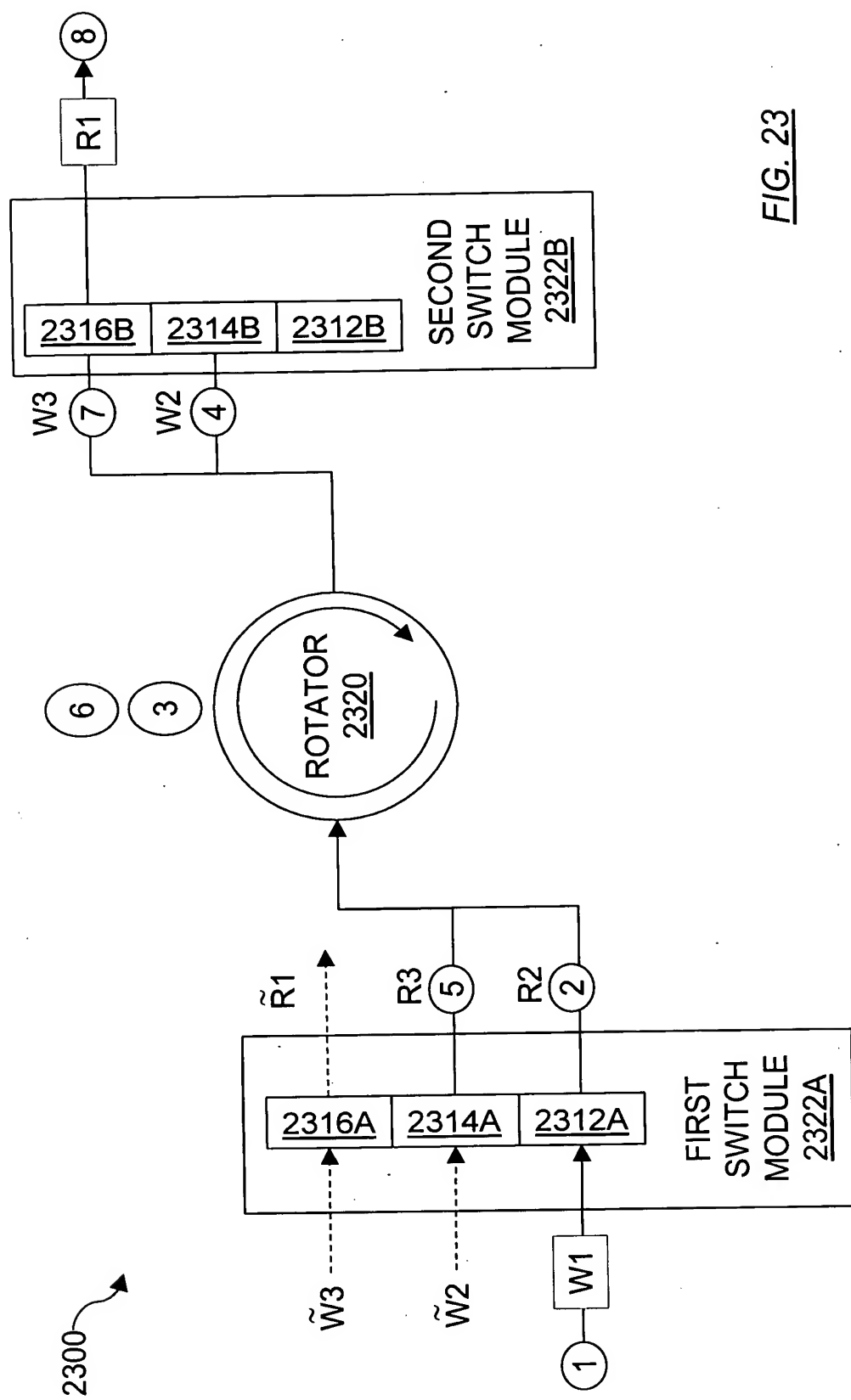


FIG. 21



PRIOR ART

FIG. 22



**FIG. 23**

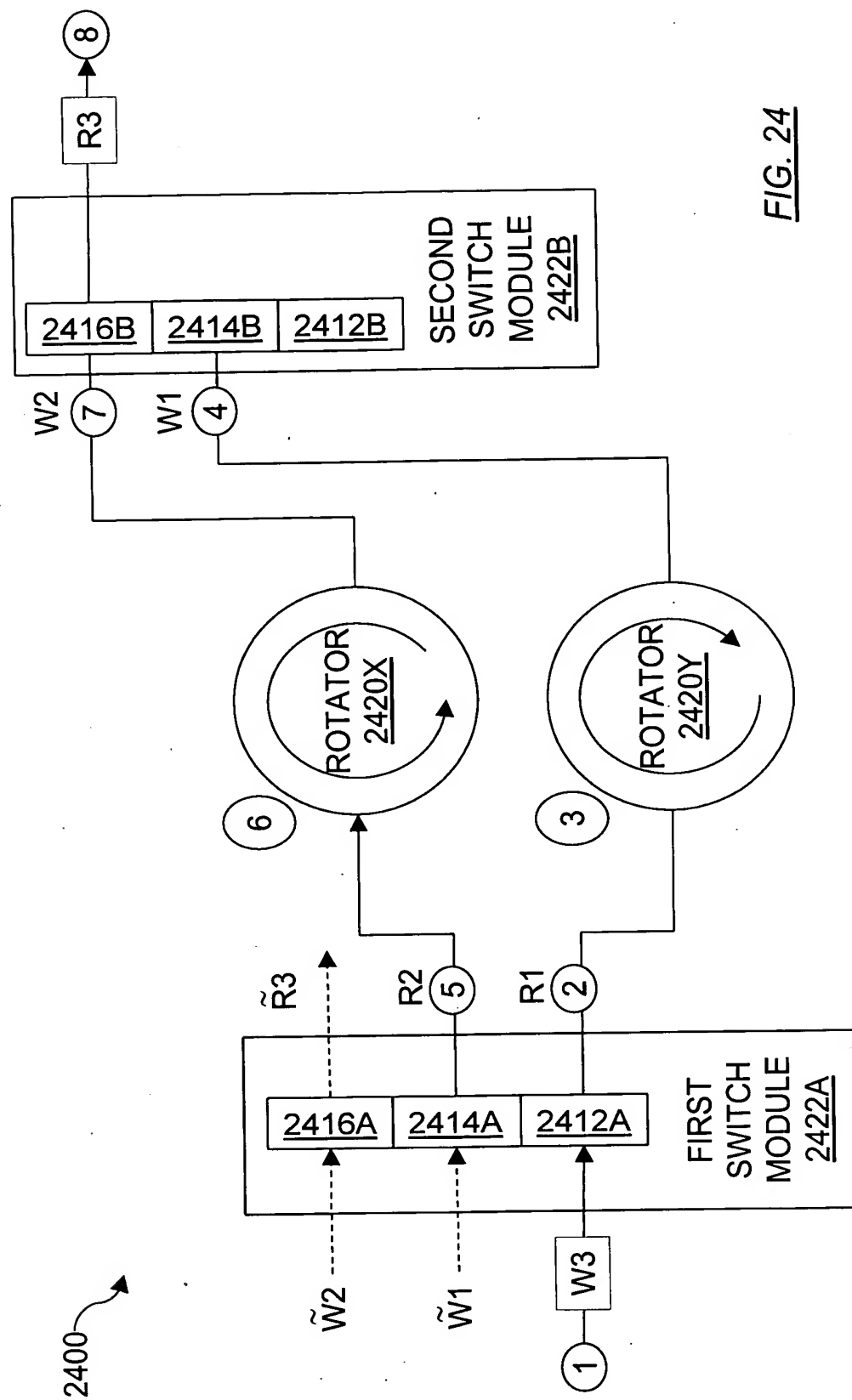


FIG. 24



PHASE-1 554

2500

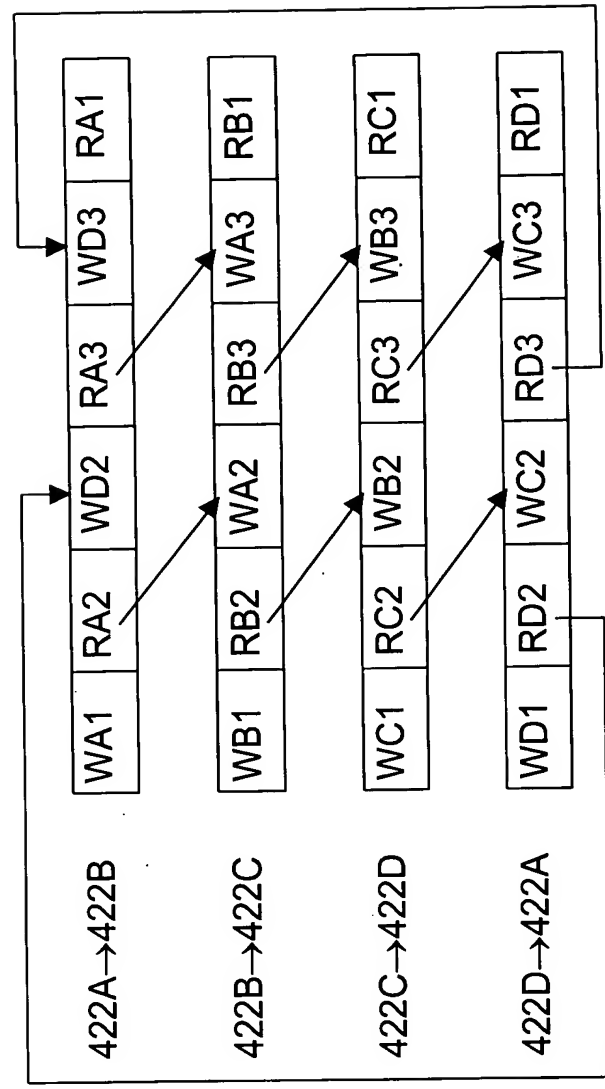


FIG. 25

PHASE-1 554

2600

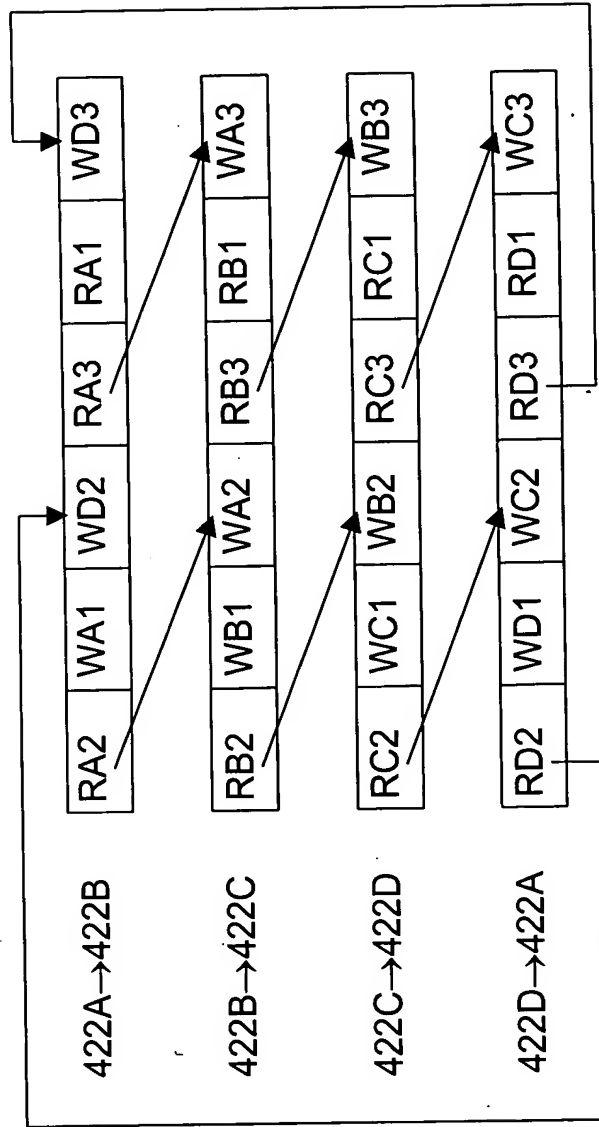


FIG. 26



Absolute time  
2812

Cyclic time  $\tau=0$  1 2 3 4 5 6 7 8 9 10 11 12 13 14 15  
2814  $t=0$  1 2 3 4 5 6 7 0 1 2 3 4 5 6 7

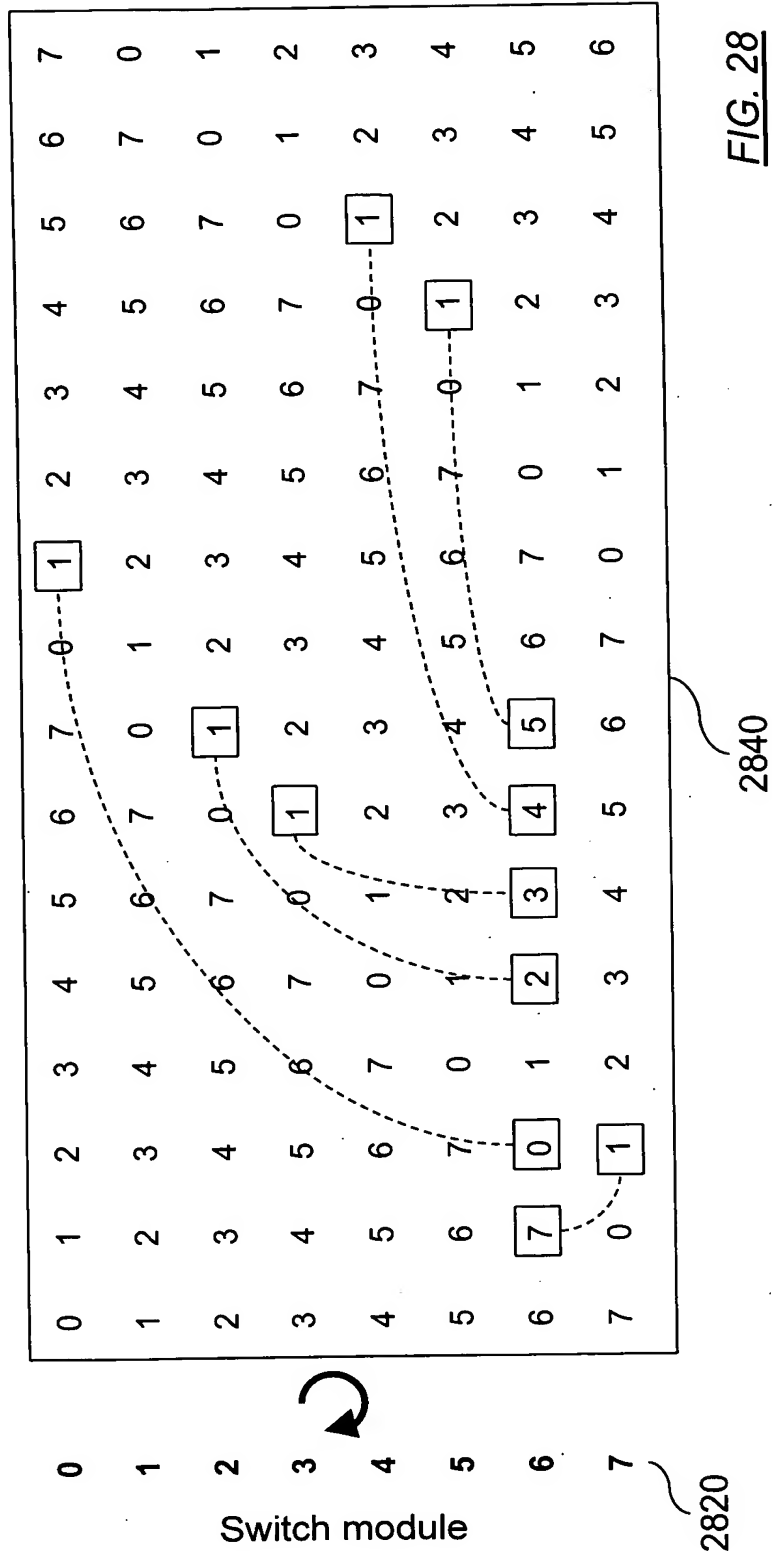


FIG. 28

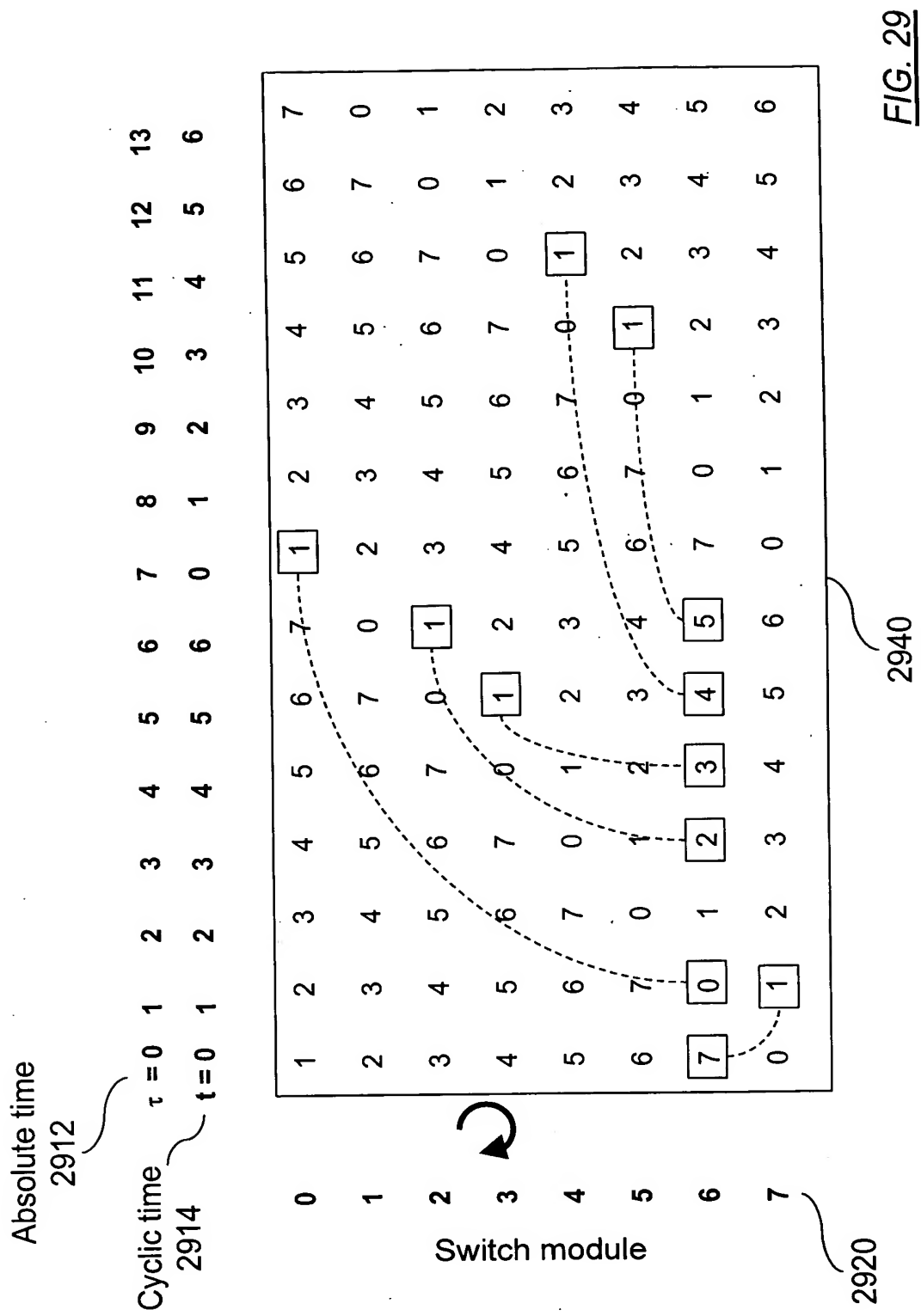


FIG. 29

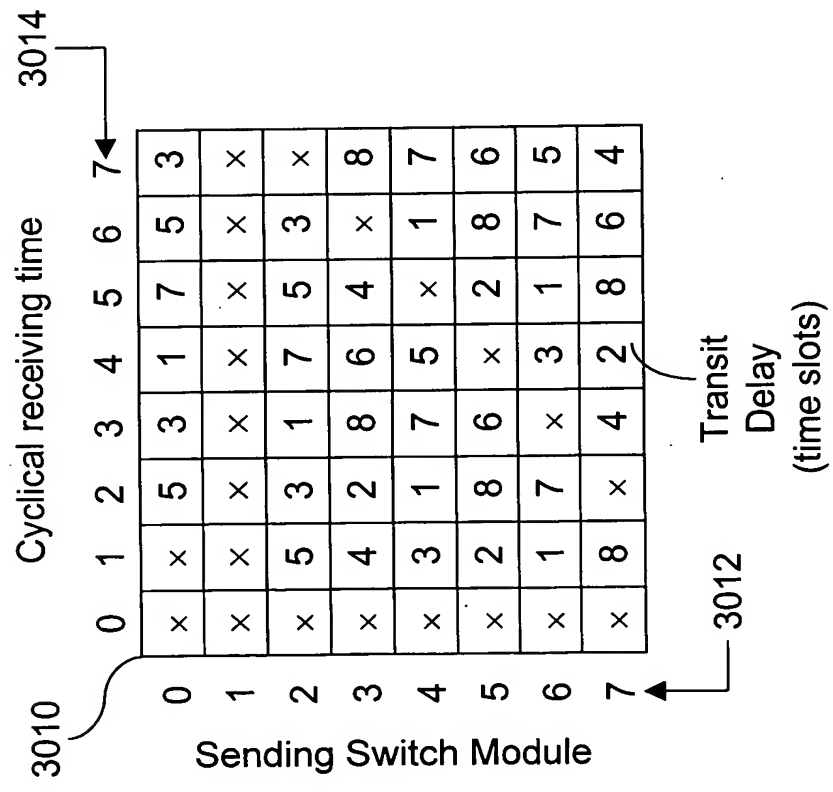
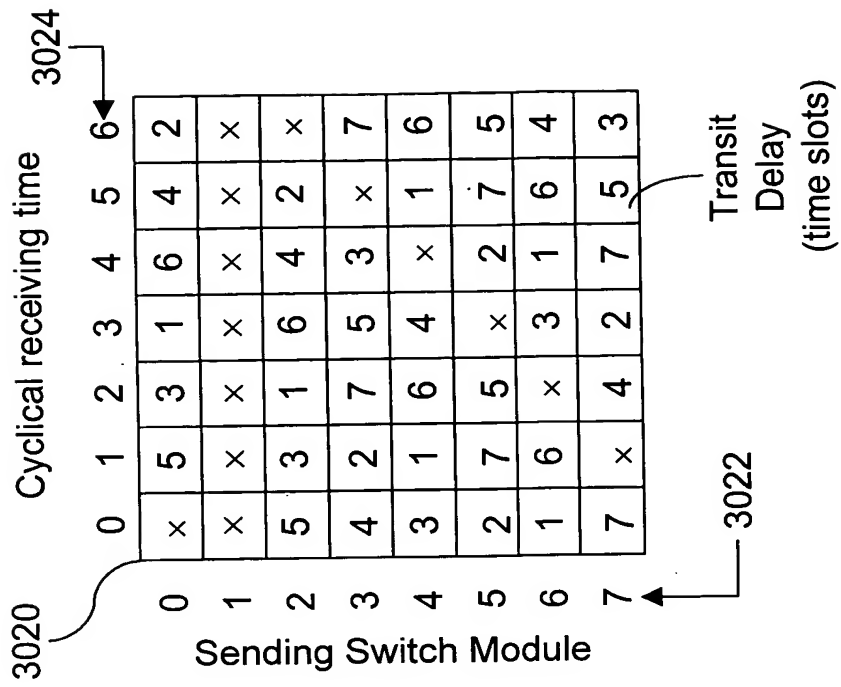


FIG. 30

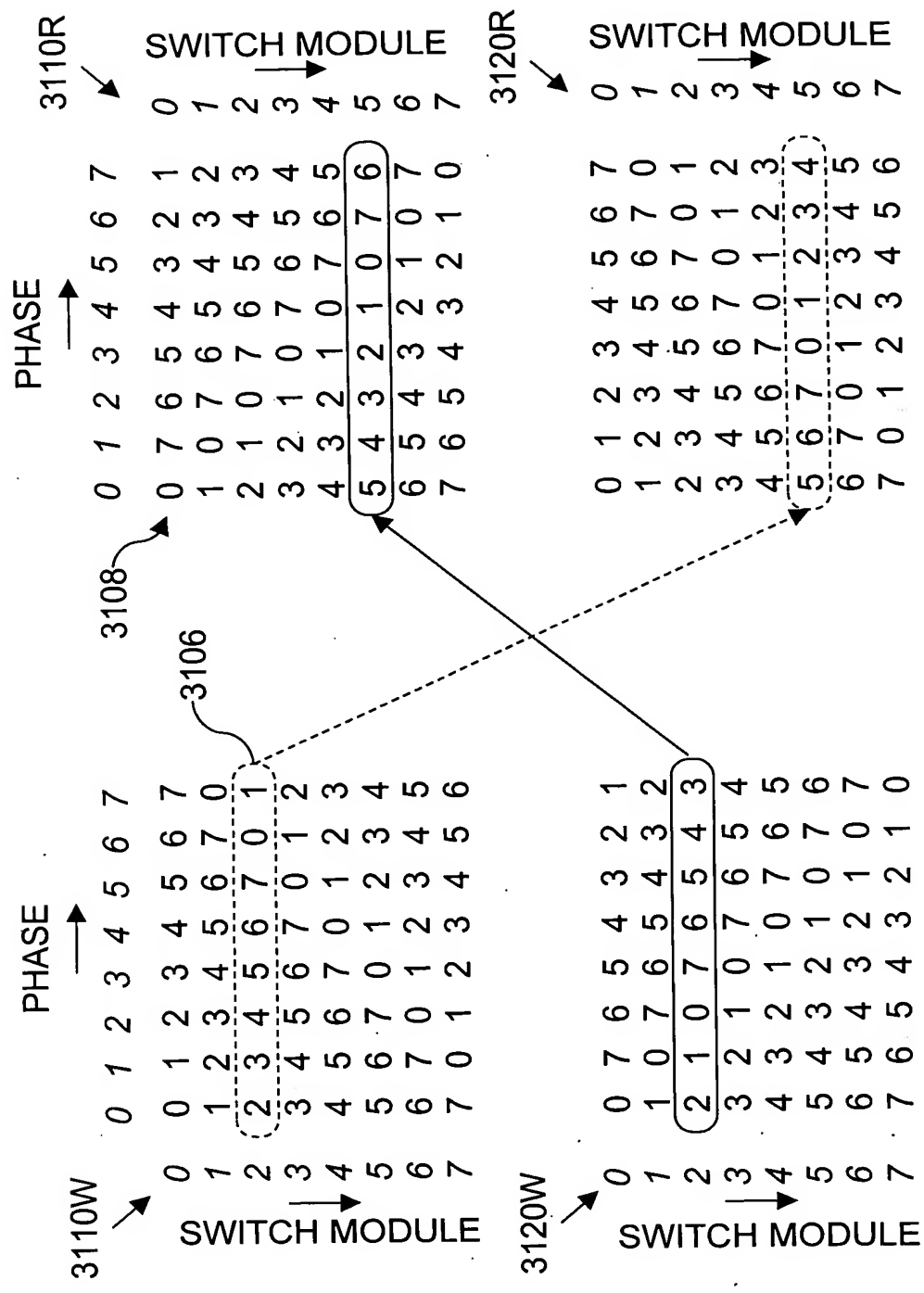


FIG. 31

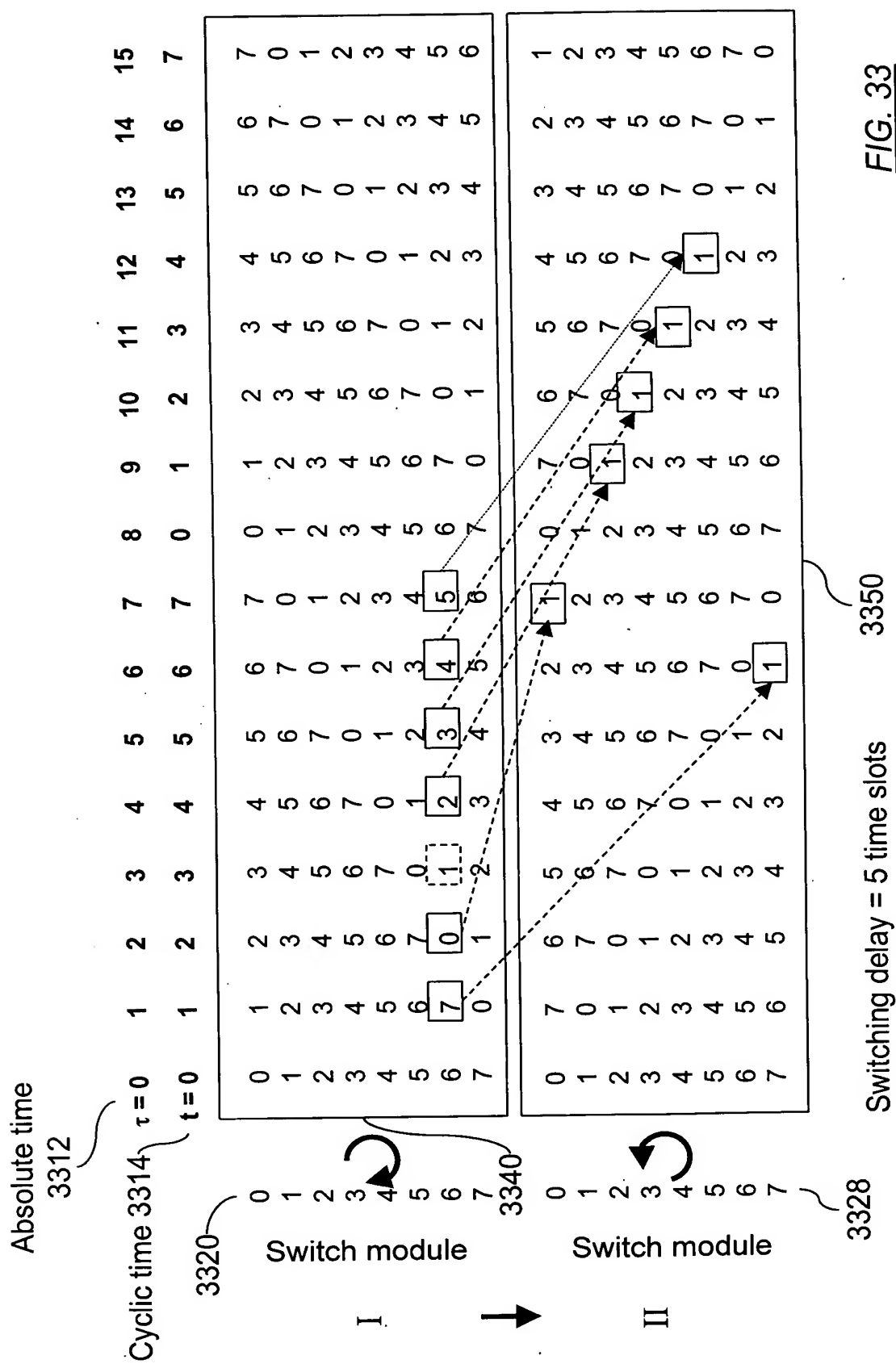
3202

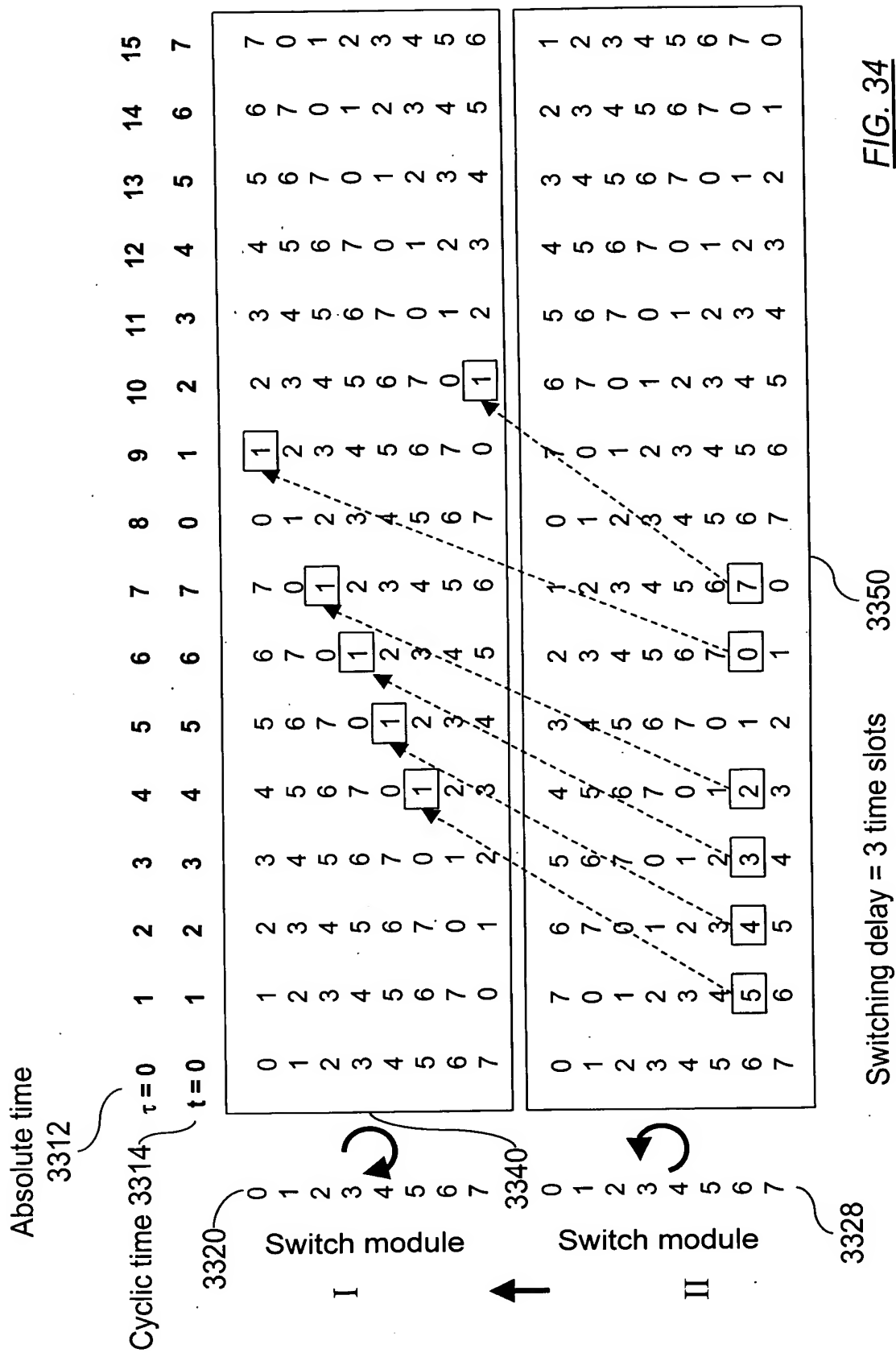
INTERMEDIATE SWITCH MODULE

	0	1	2	3	4	5	6	7	
									3210F
Data Segment Receipt Phase (First rotator)	6	7	0	1	2	3	4	5	
									3212F
Data Segment Transmission Phase (First rotator)	5	4	3	2	1	0	7	6	
									3210S
Data Segment Receipt Phase (Second rotator)	2	1	0	7	6	5	4	3	
									3212S
Data Segment Transmission Phase (Second rotator)	3	4	5	6	7	0	1	2	
<hr/>									
Transit Delay (First rotator then Second rotator)	5	5	X	5	5	X	5	5	3214FS
Transit Delay (Second rotator then First rotator)	3	3	X	3	3	X	3	3	3214SF

FIG. 32







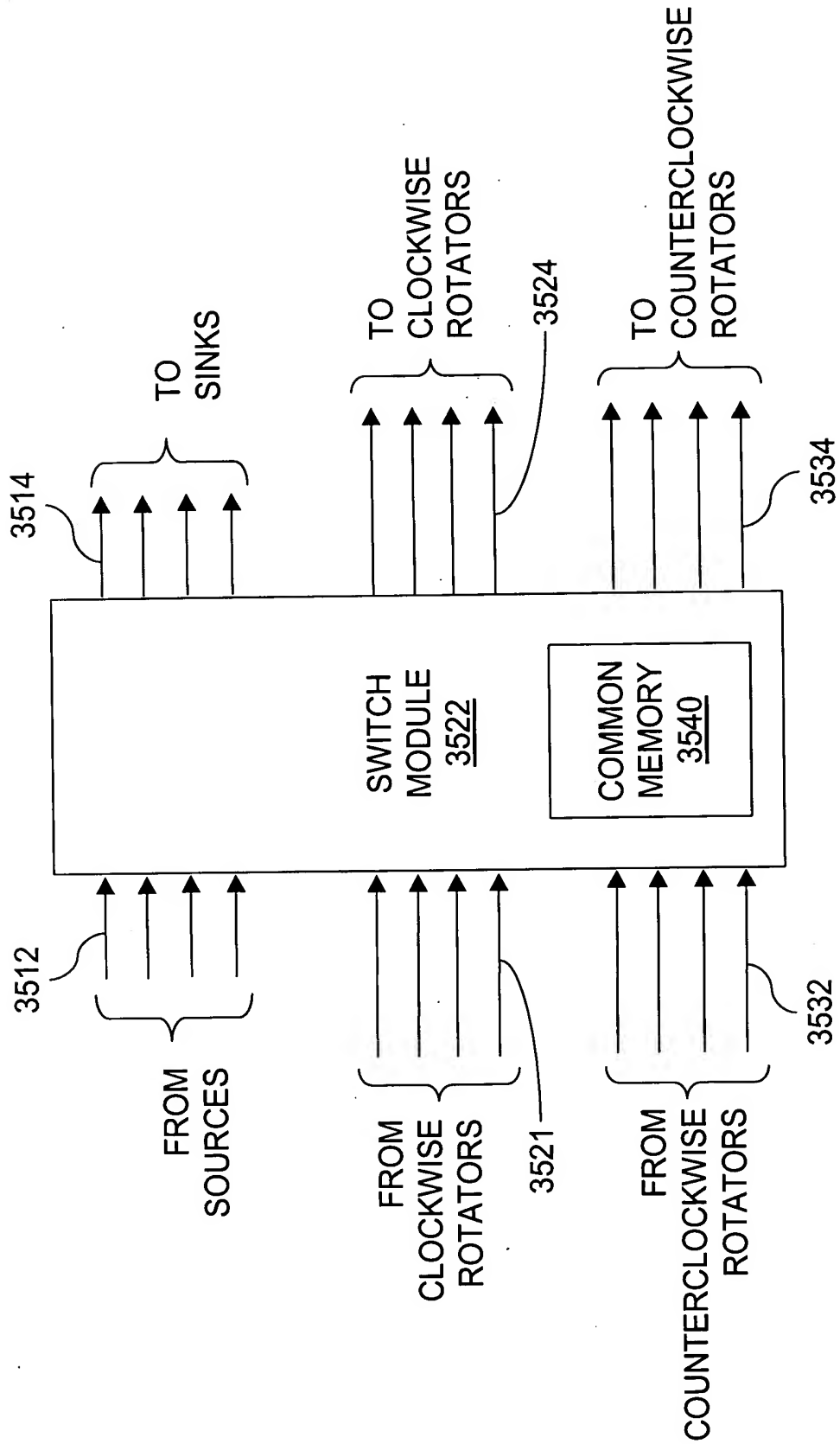


FIG. 35

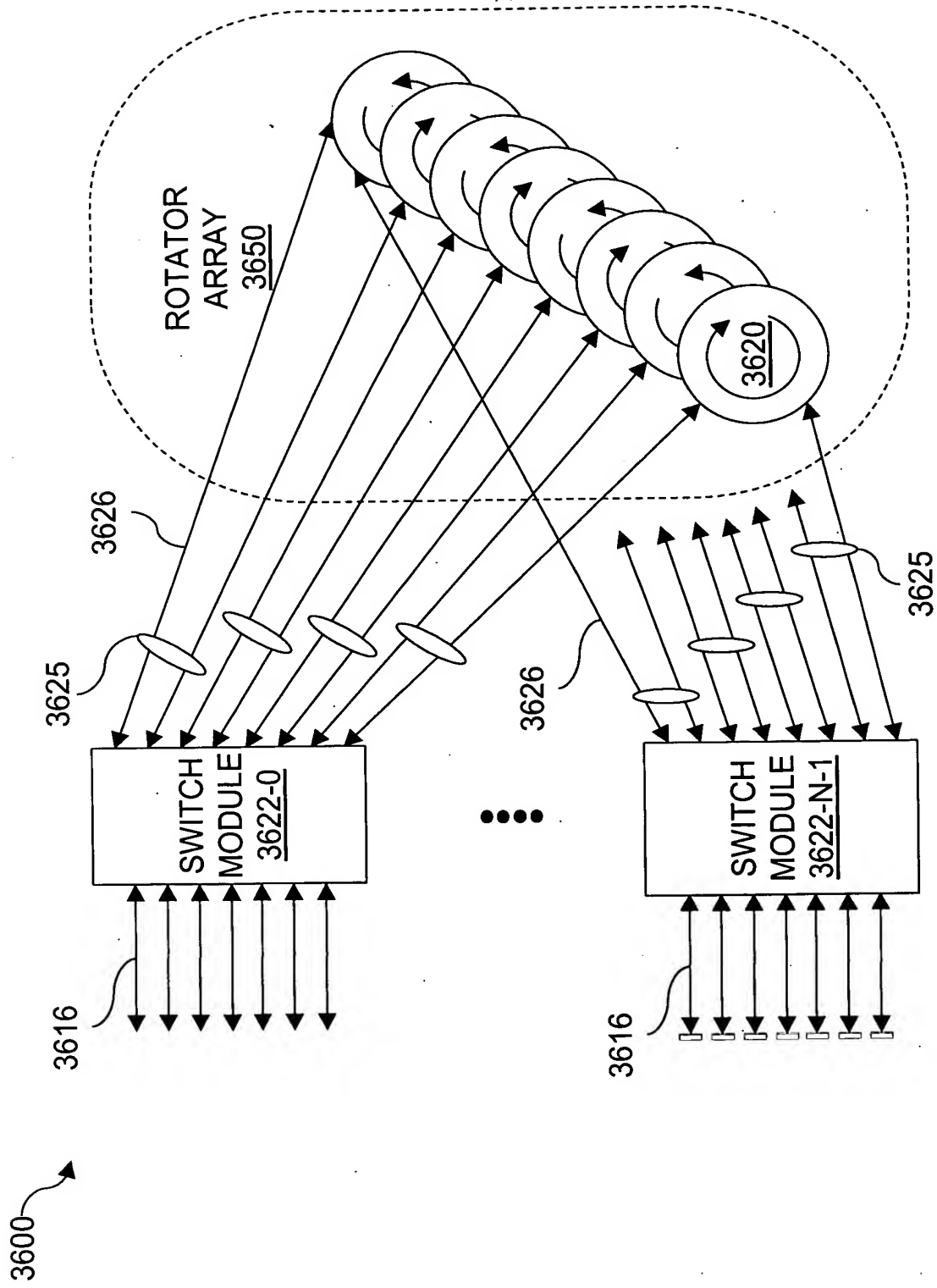


FIG. 36

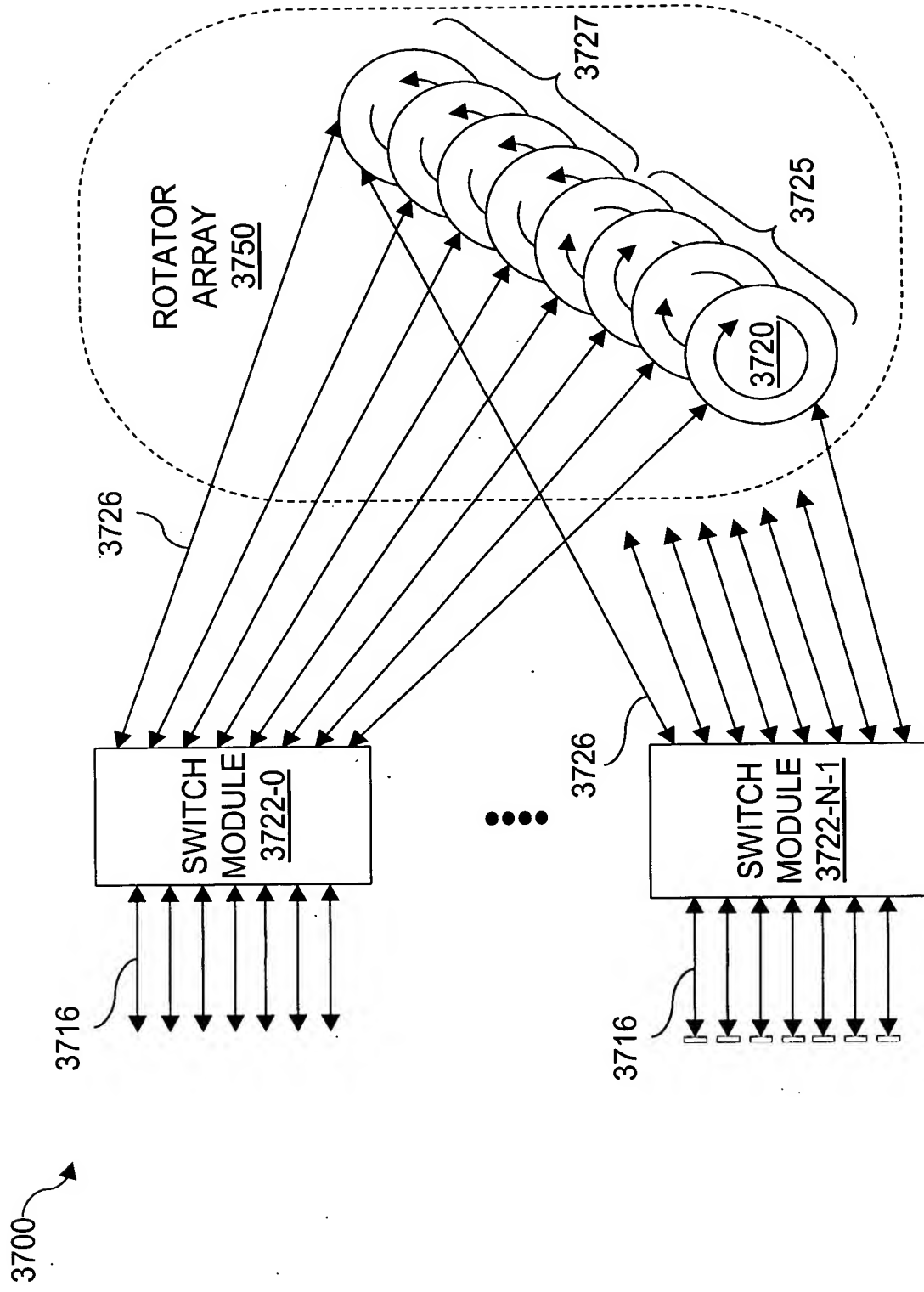


FIG. 37

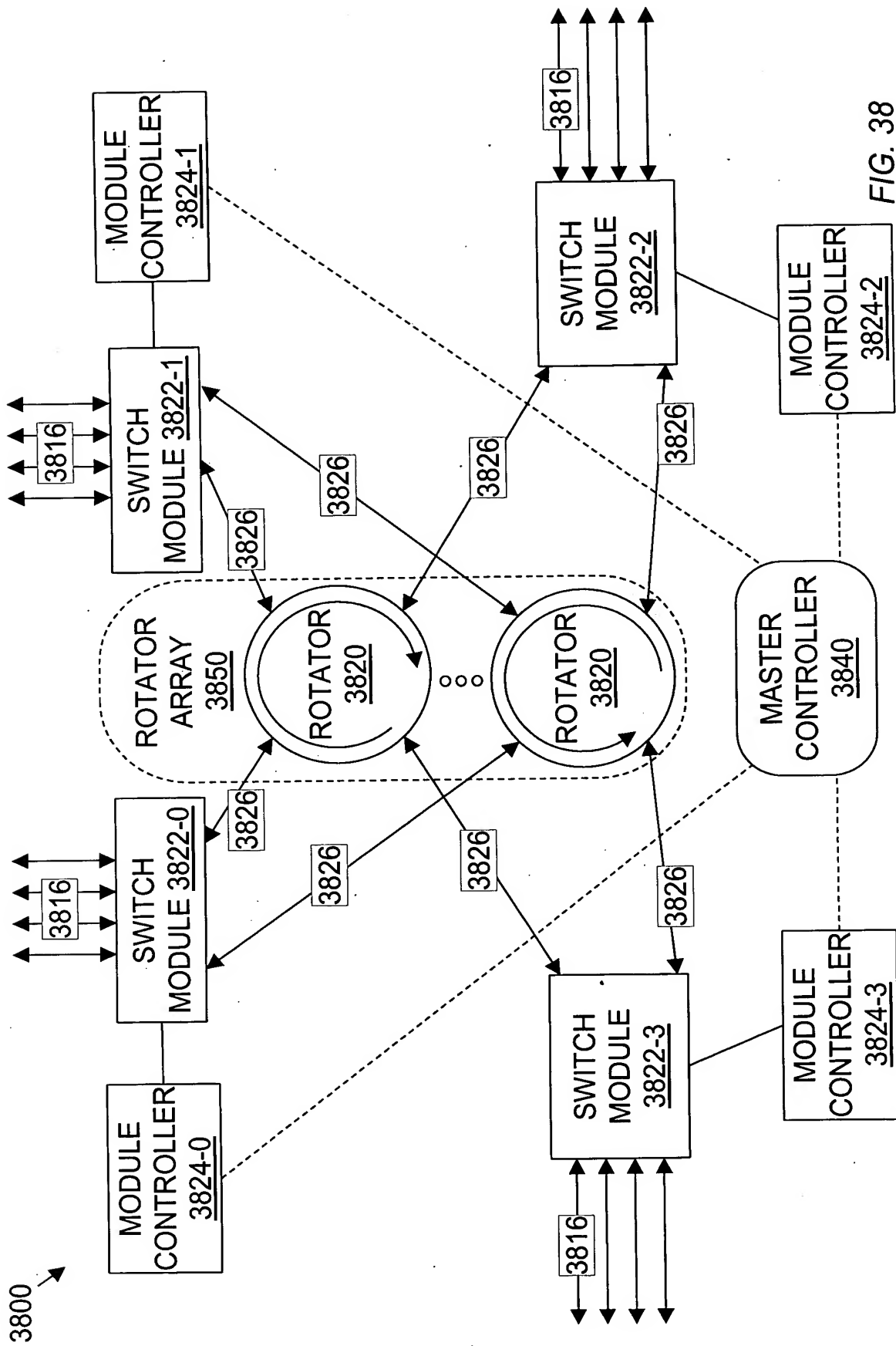
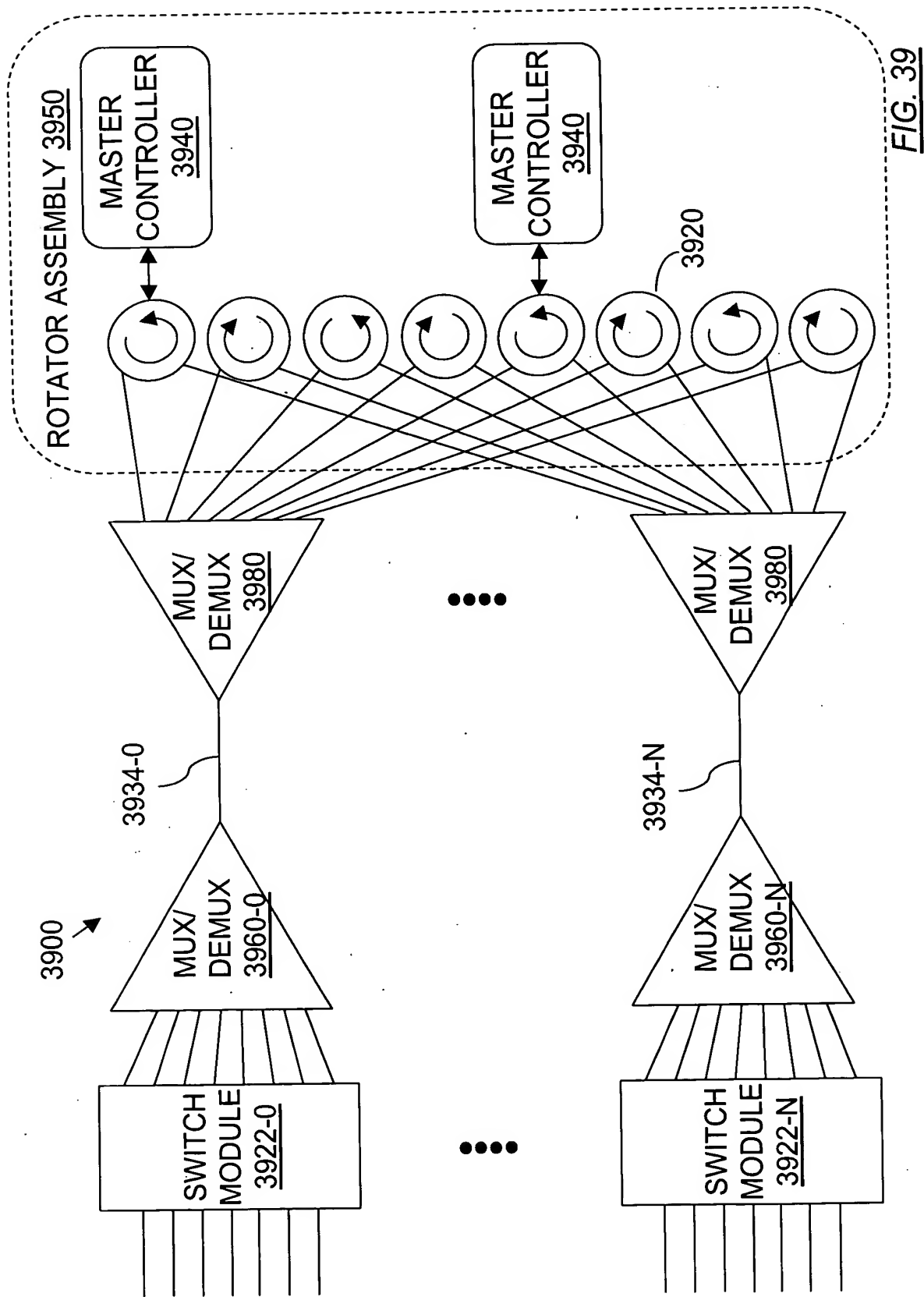


FIG. 38



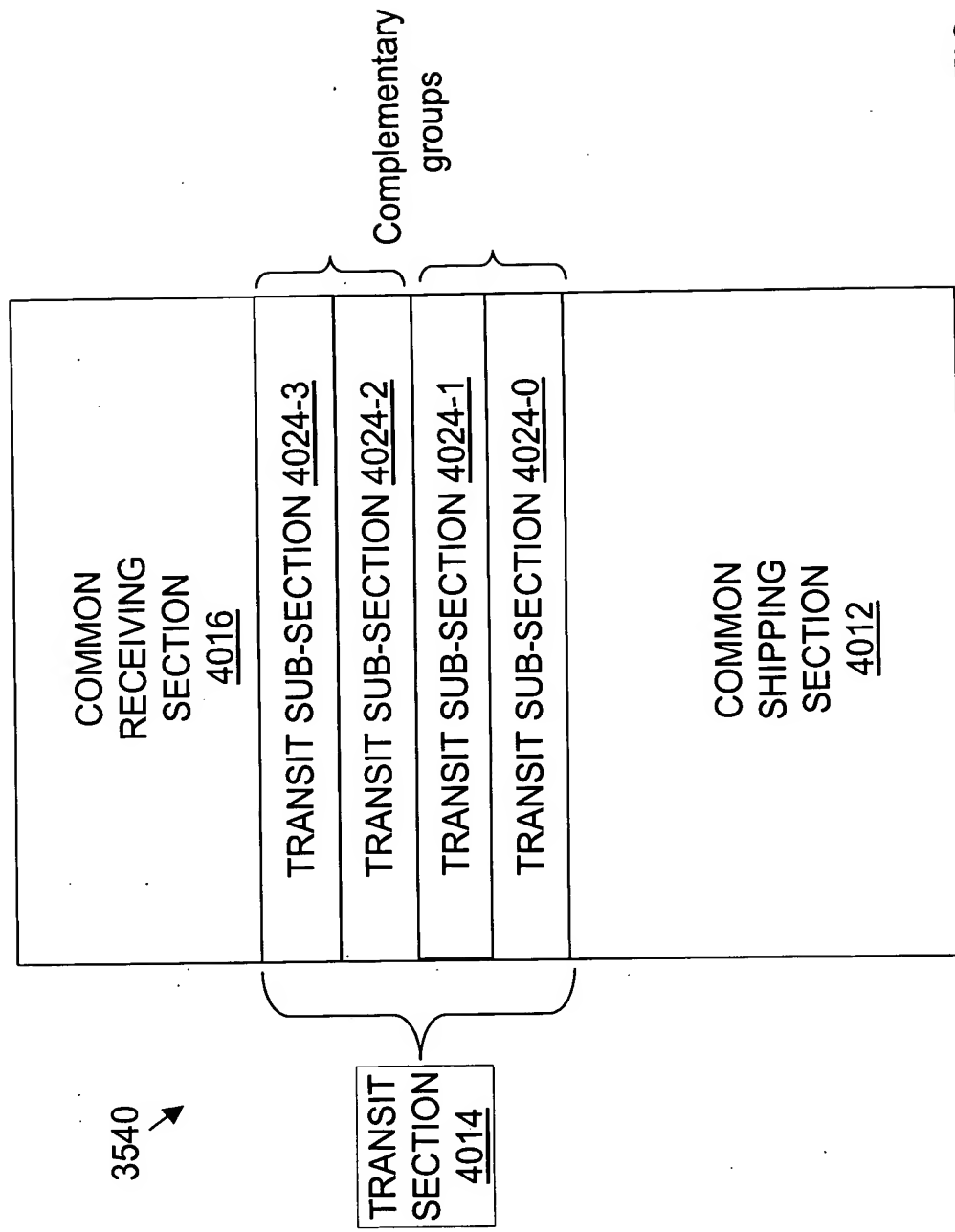


FIG. 40



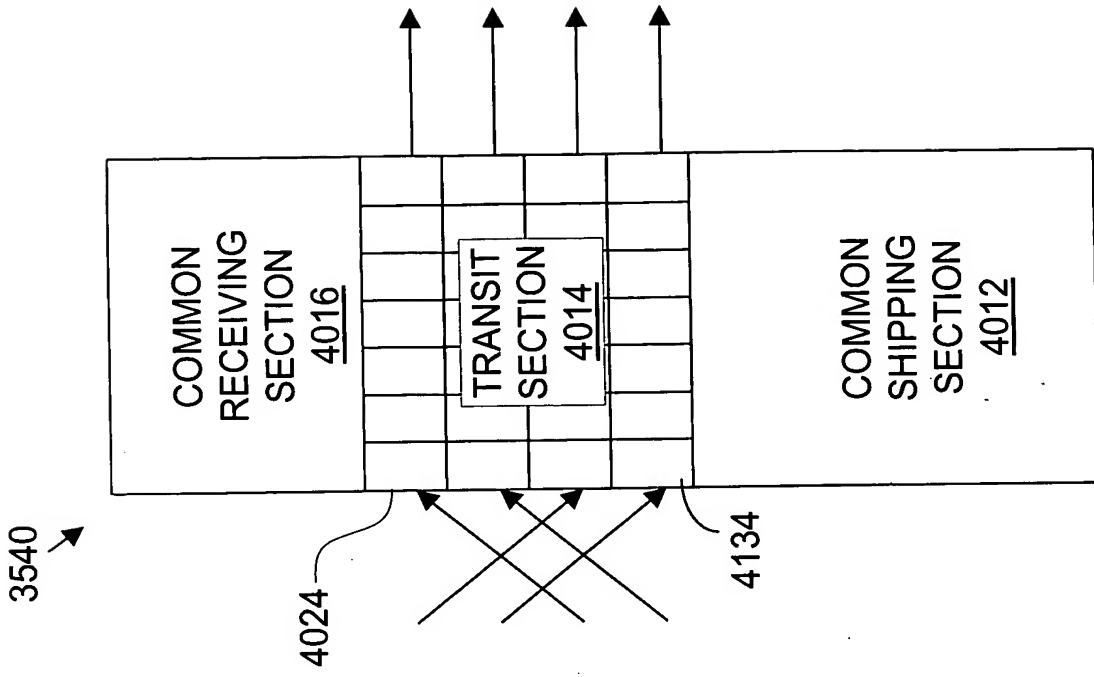


FIG. 41A

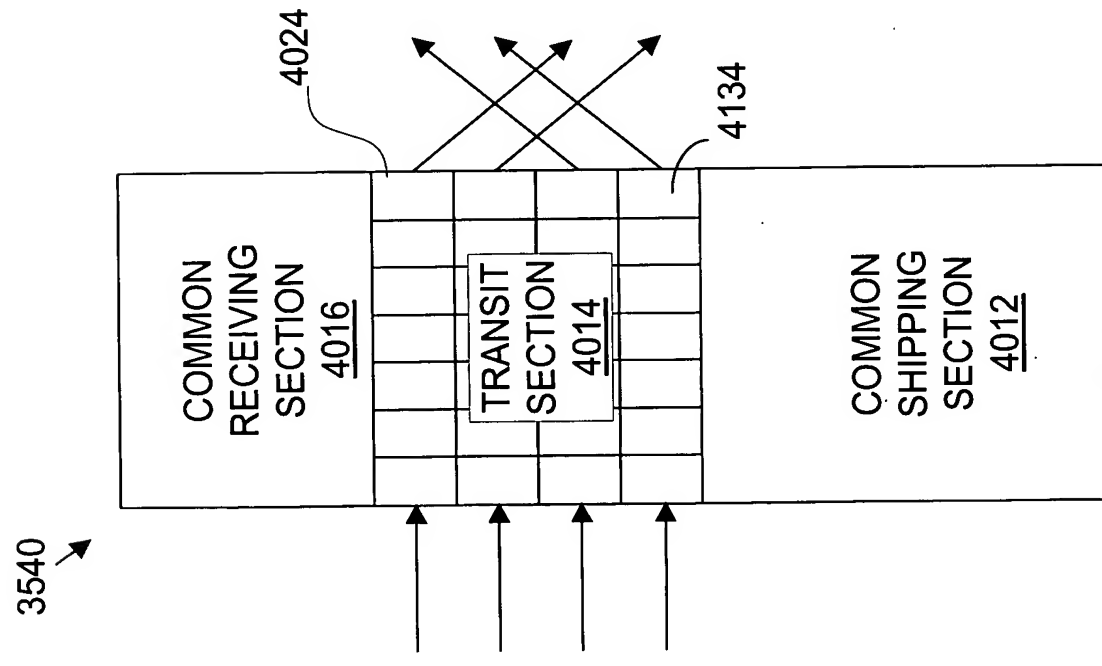
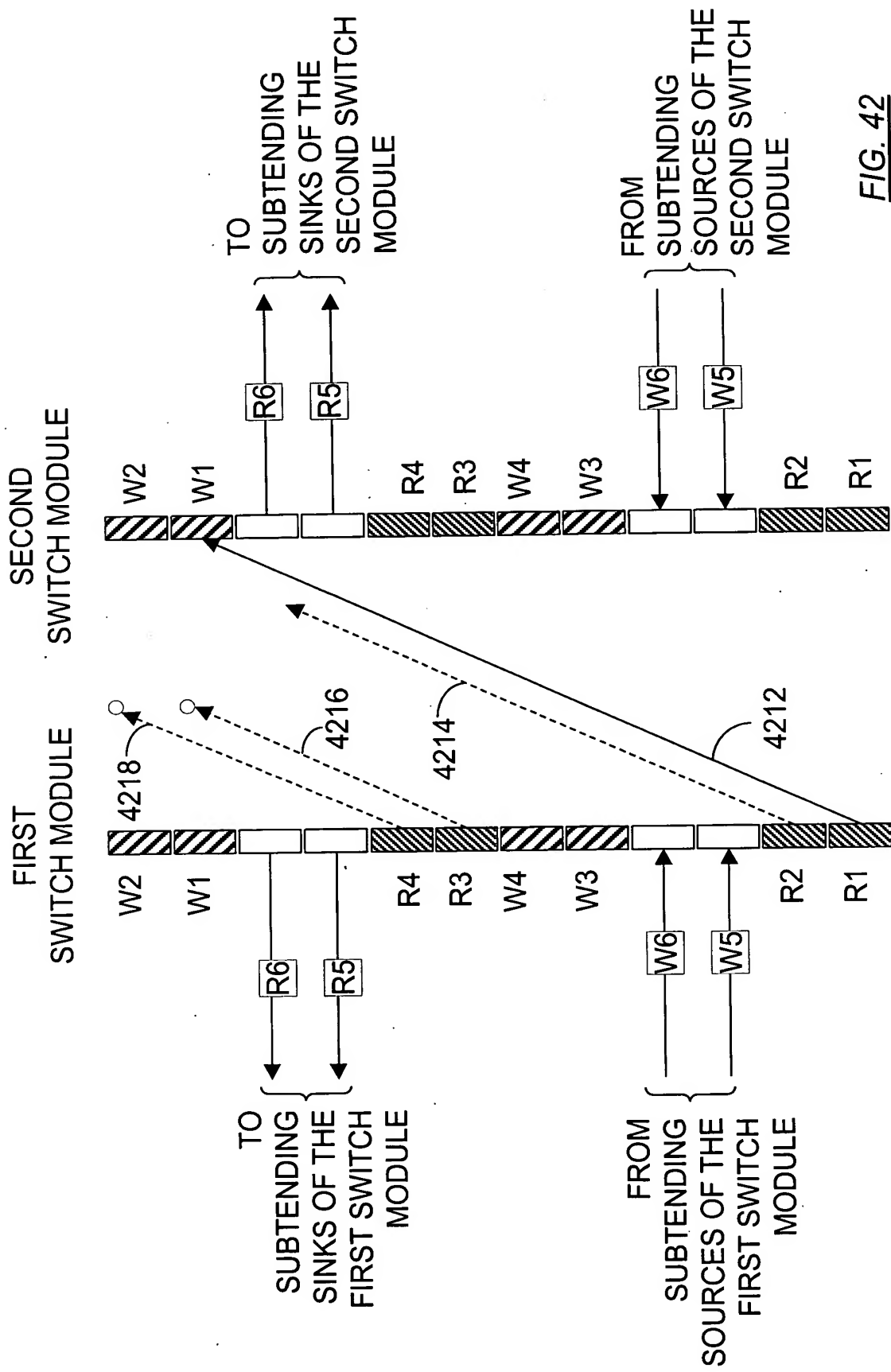
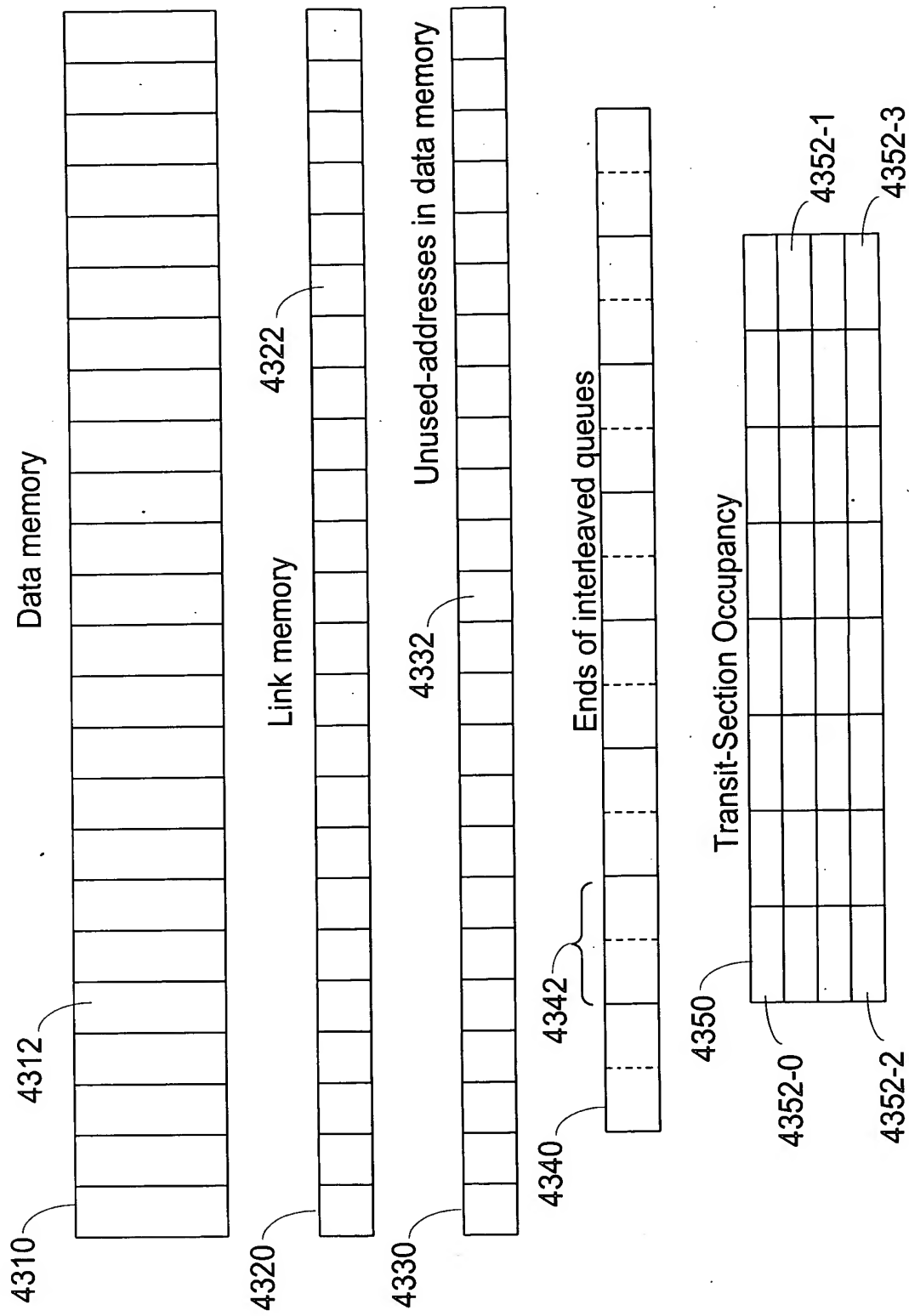


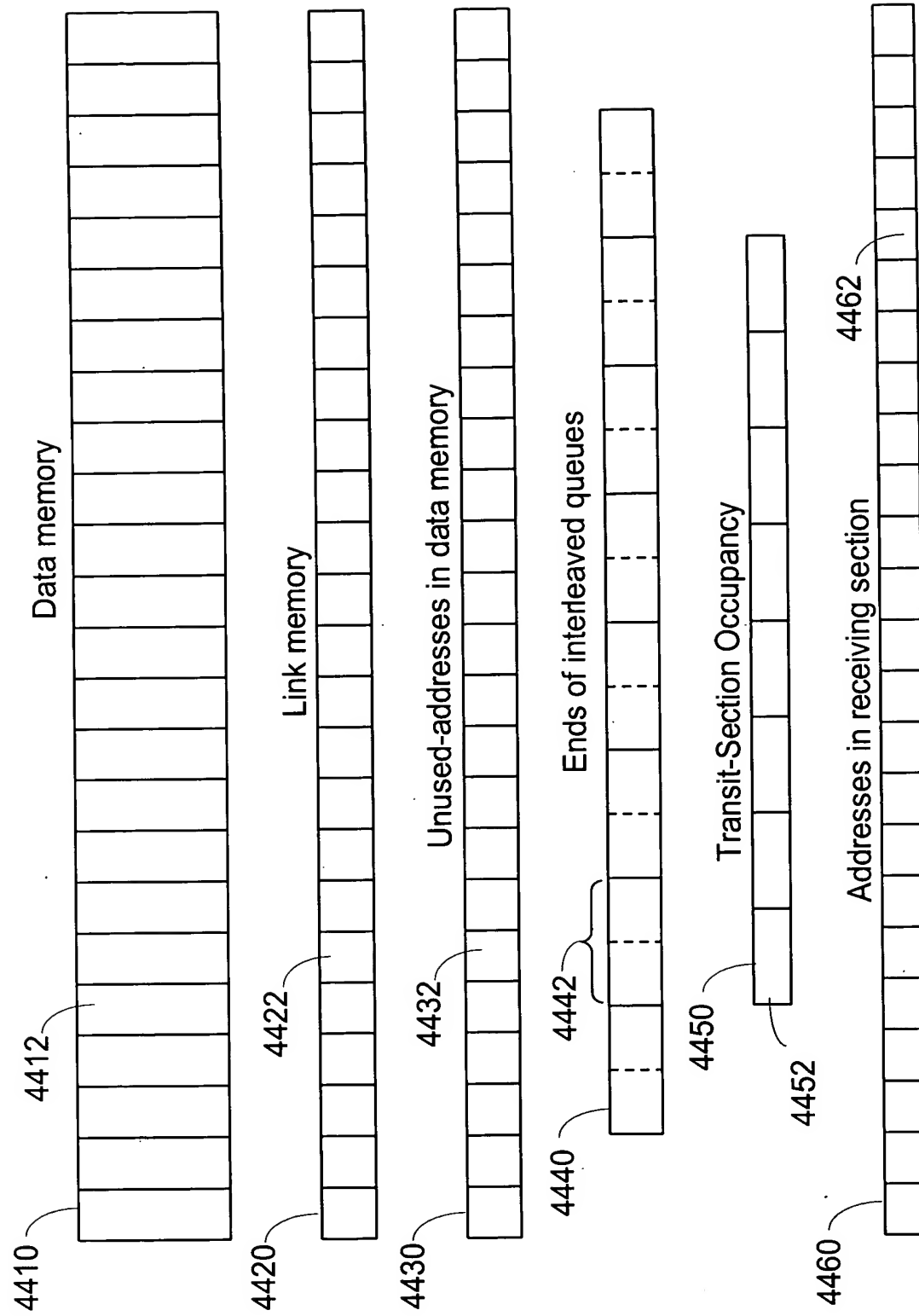
FIG. 41B



**FIG. 42**



**FIG. 43**



**FIG. 44**

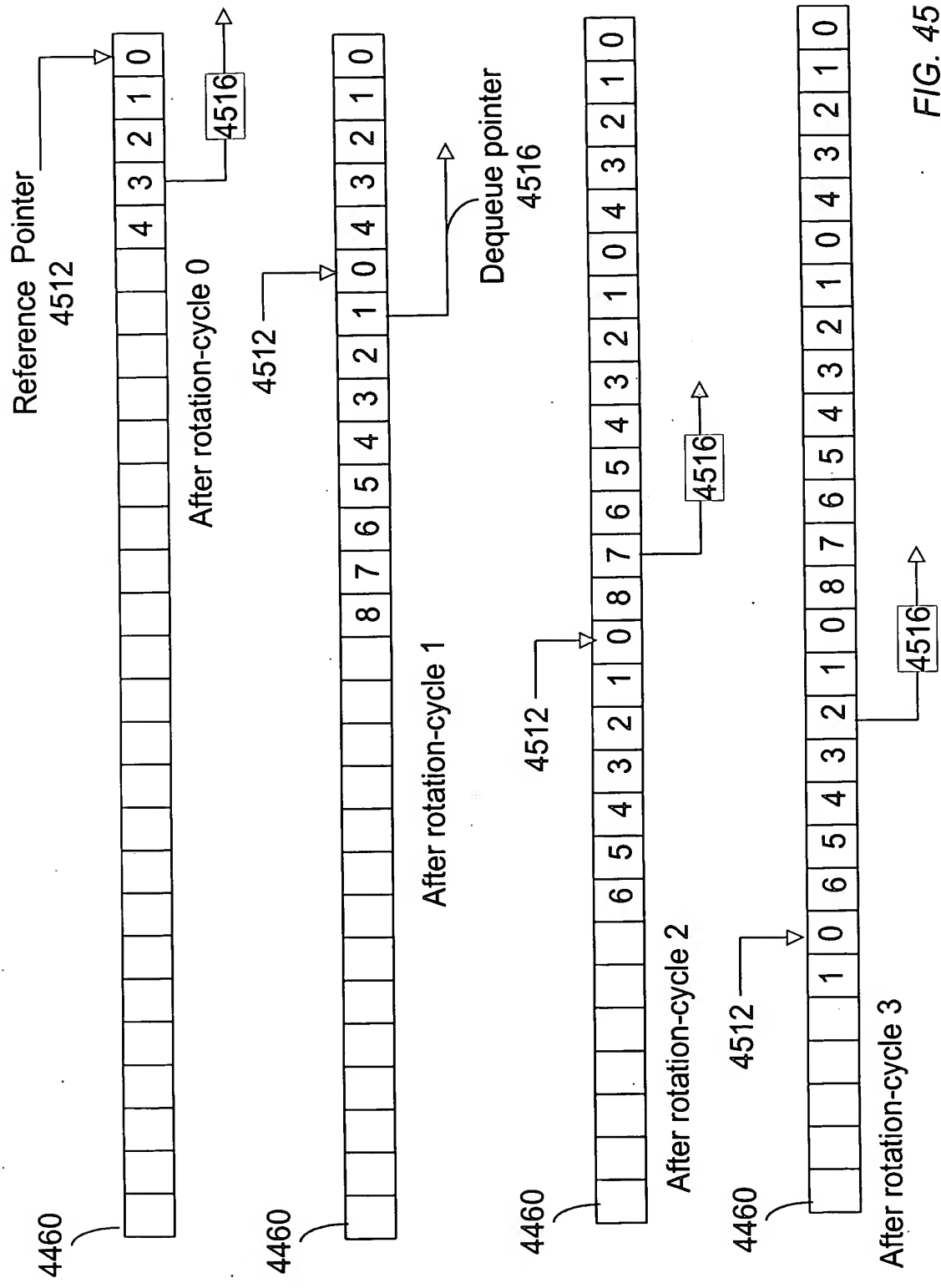


FIG. 45

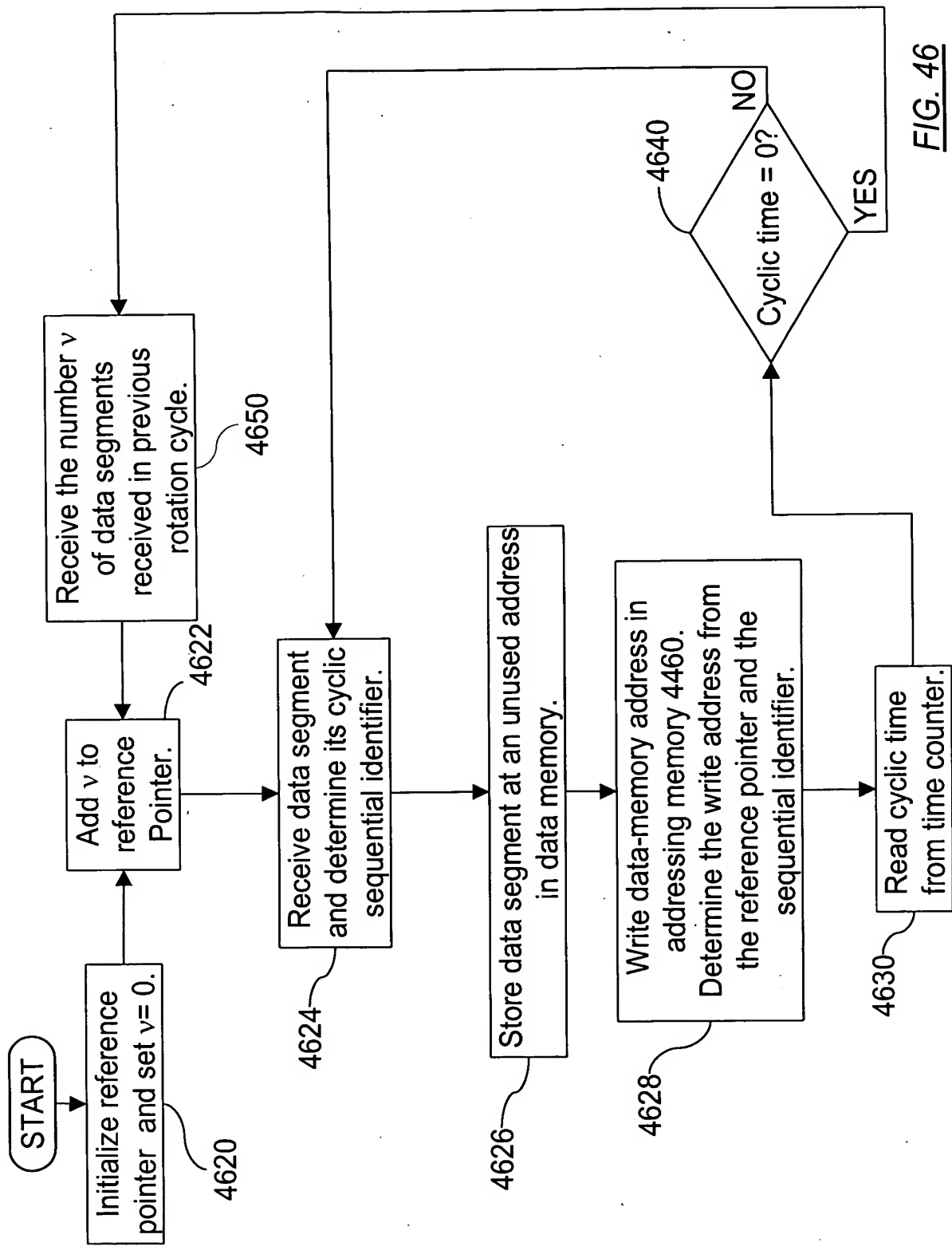
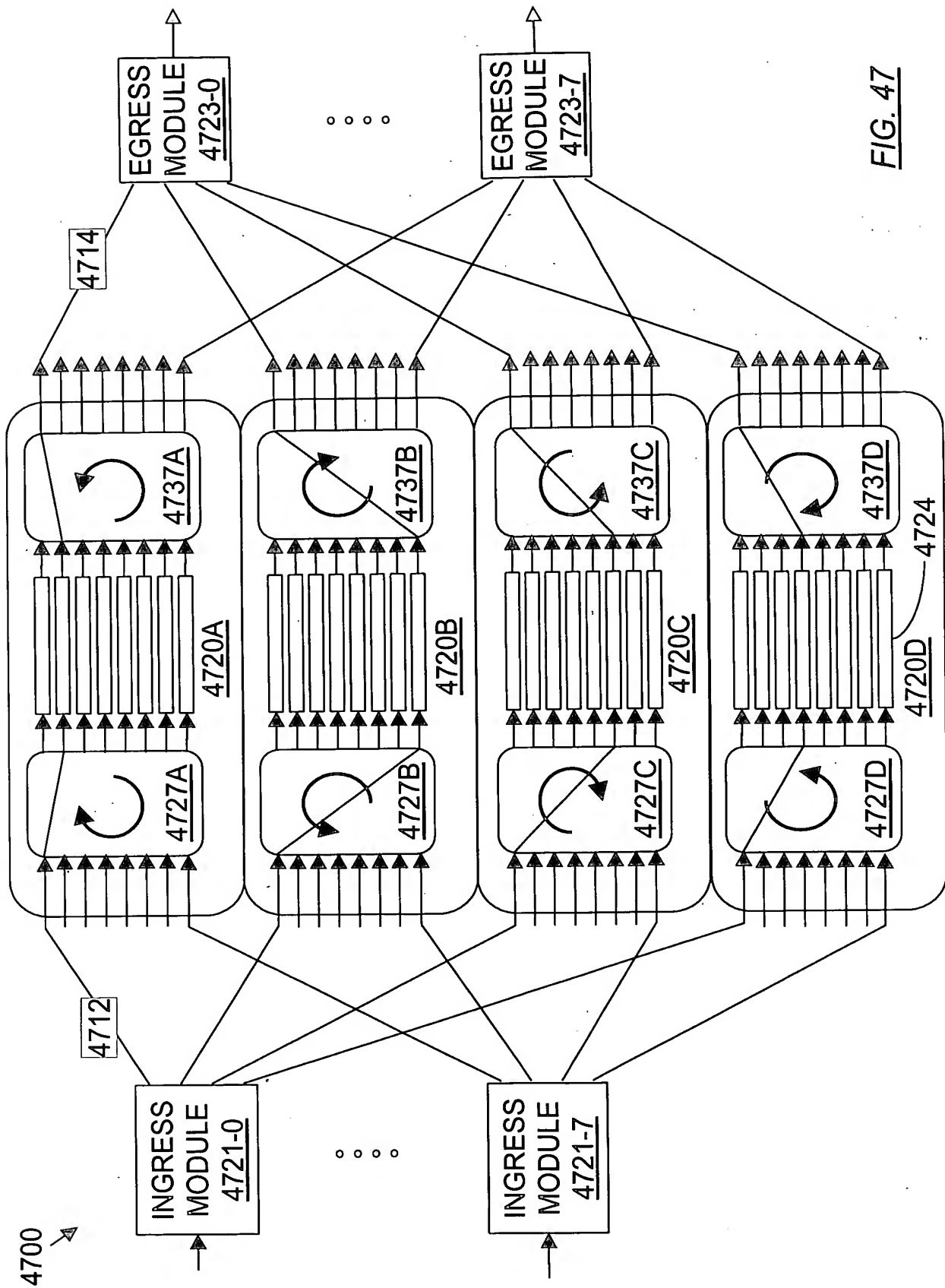


FIG. 46



**FIG. 47**

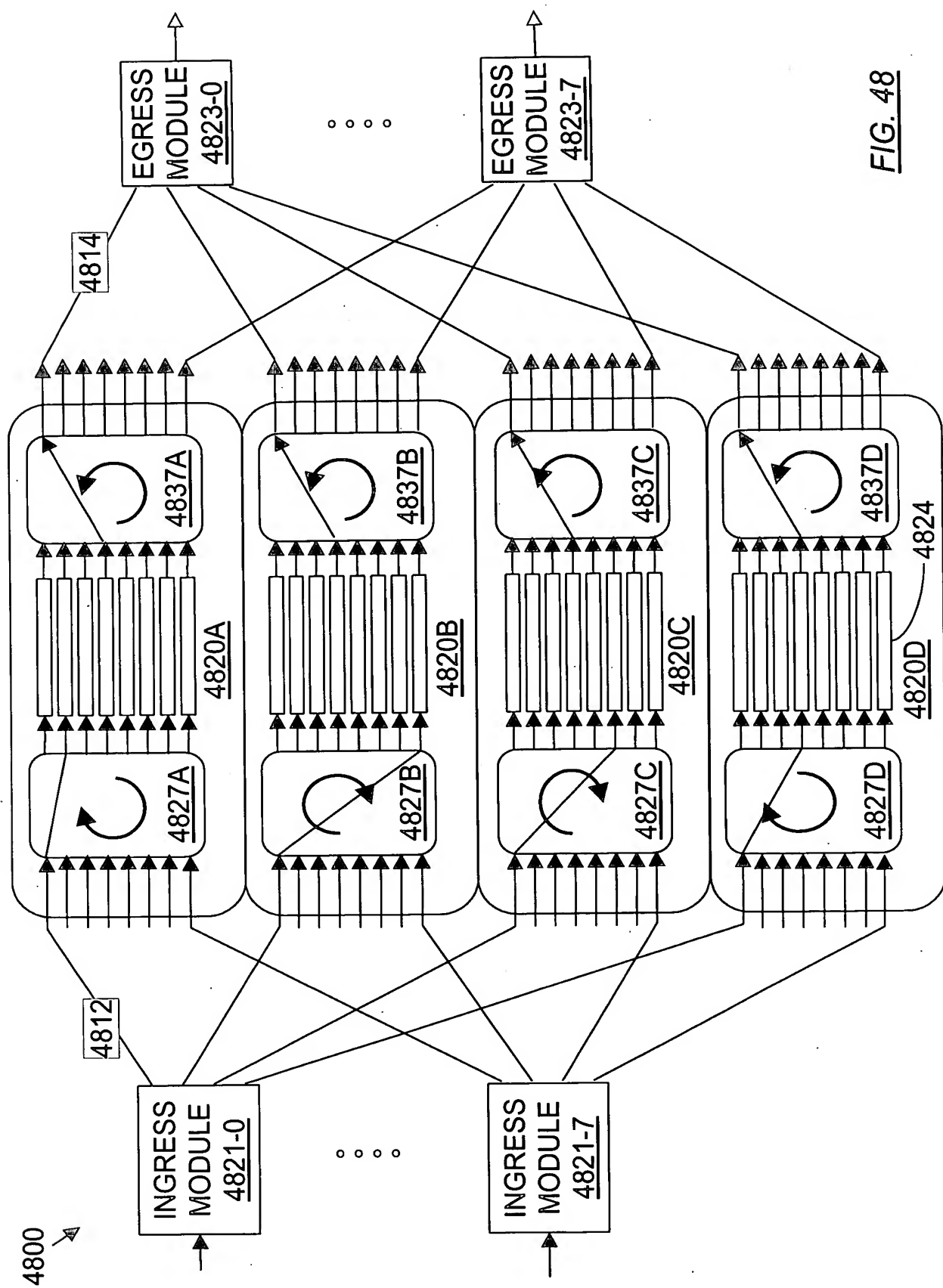


FIG. 48



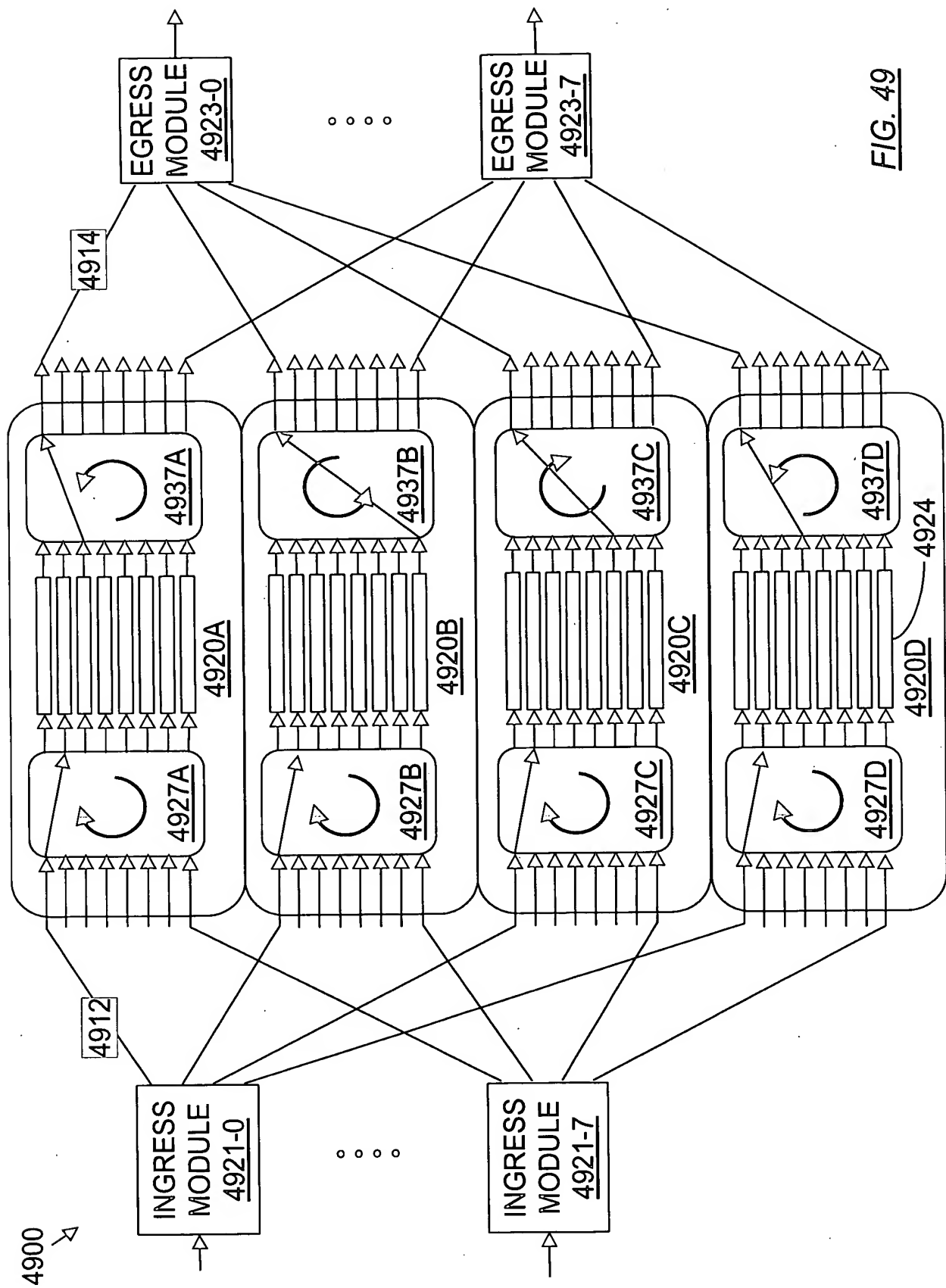


FIG. 49

5000

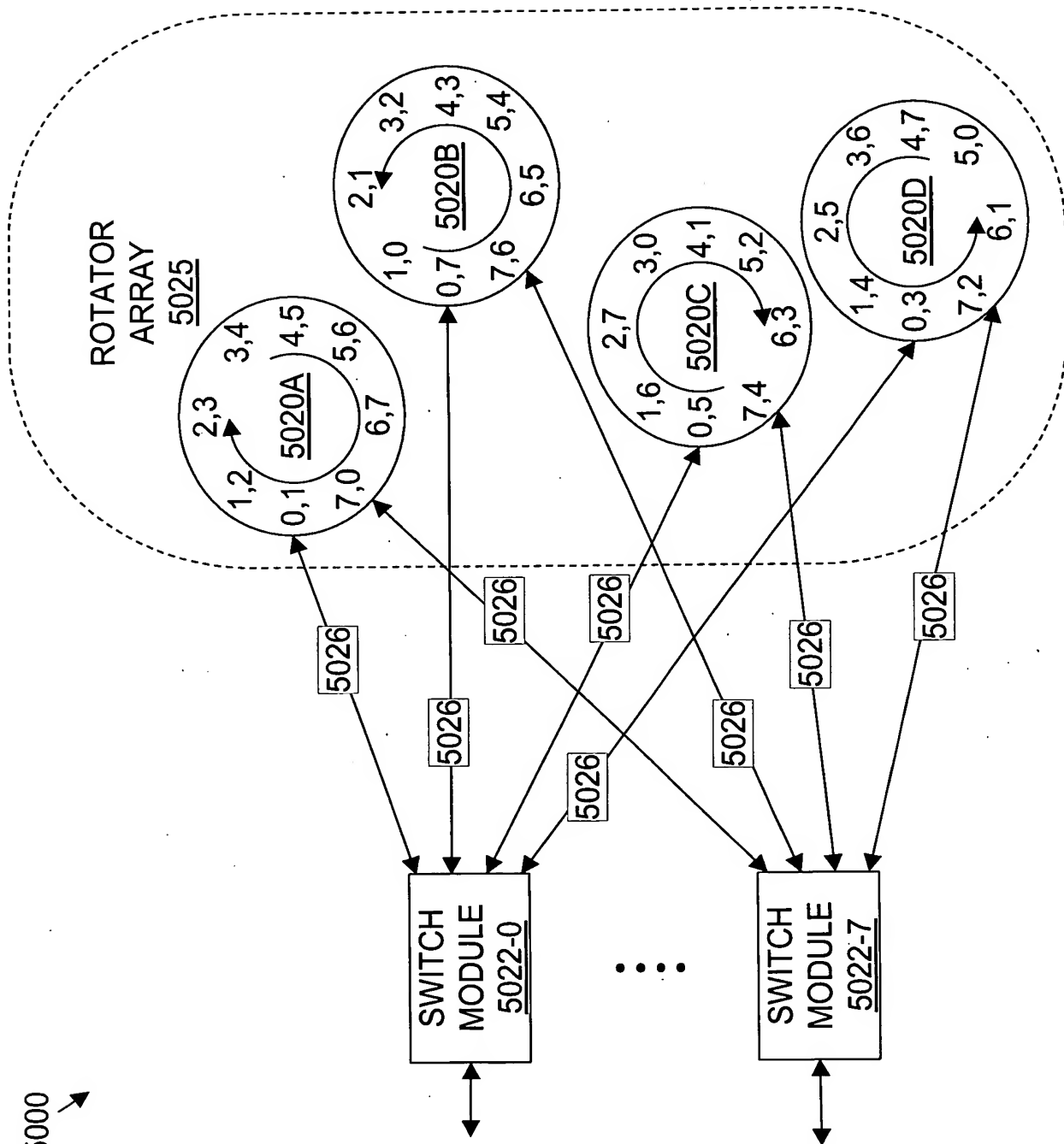


FIG. 50

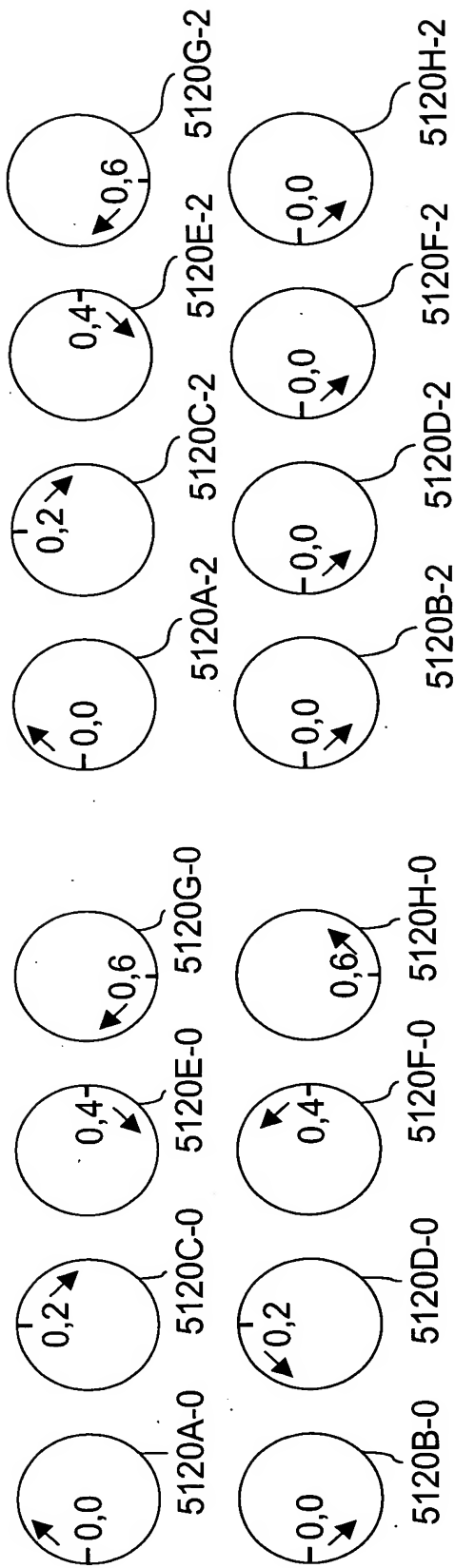


FIG. 51A

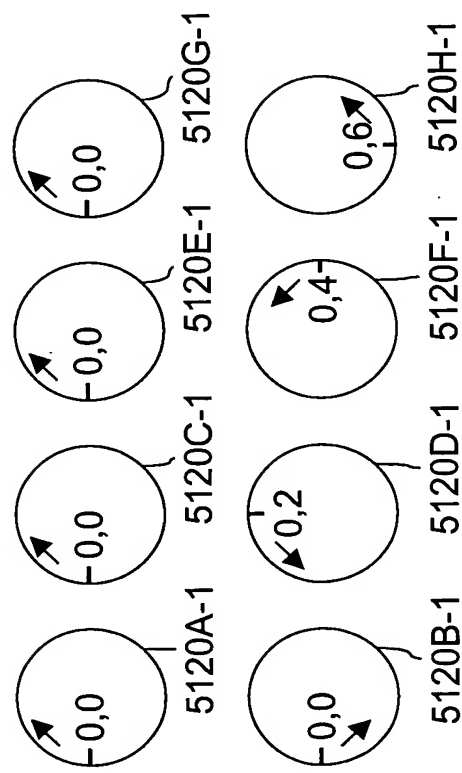


FIG. 51B

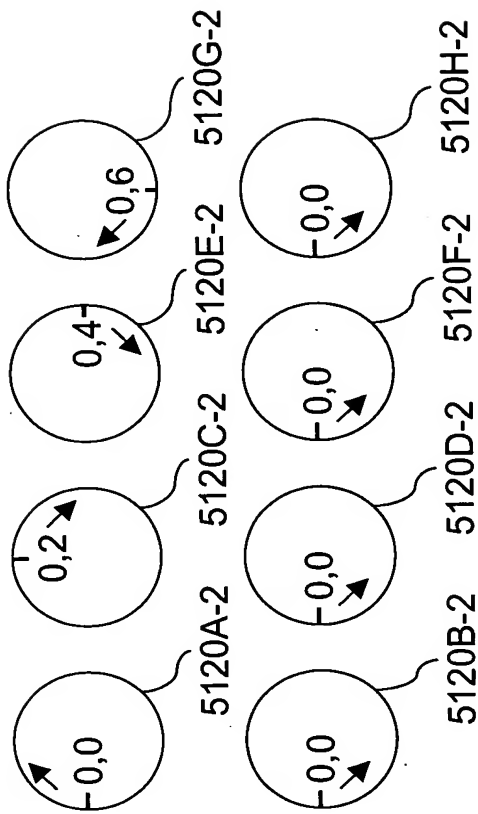


FIG. 51C

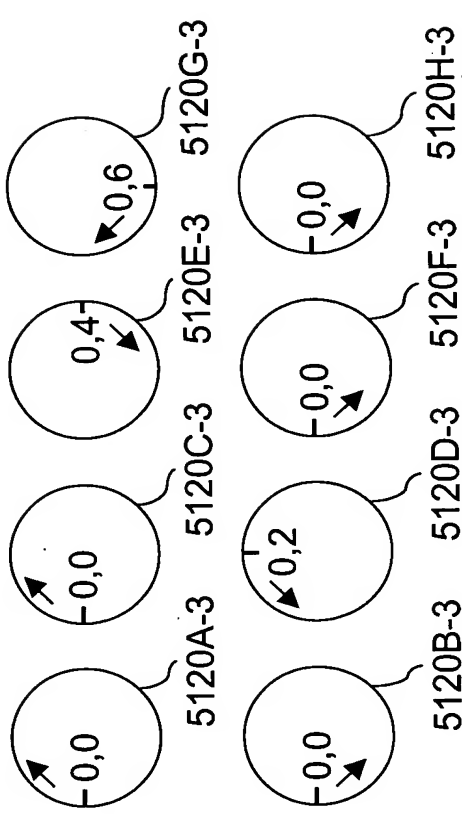


FIG. 51D

ROTATION PHASE  $t = 0$  ( $T=8$ )

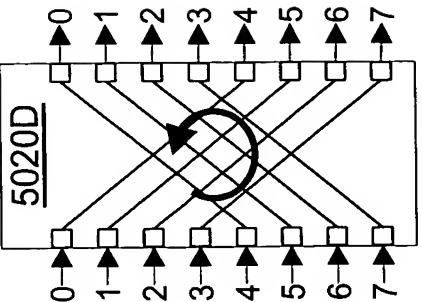
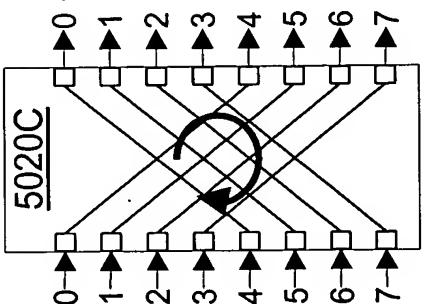
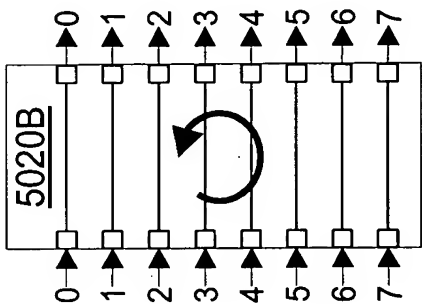
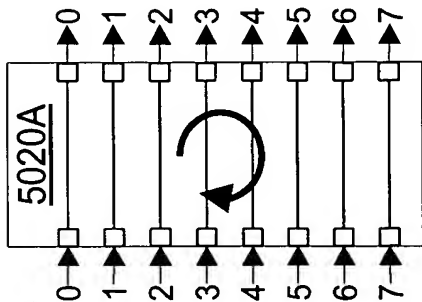


FIG. 52A

ROTATION PHASE  $t = 6$  ( $T=8$ )

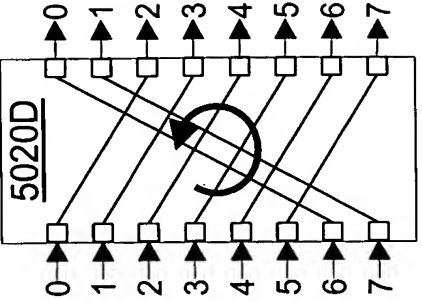
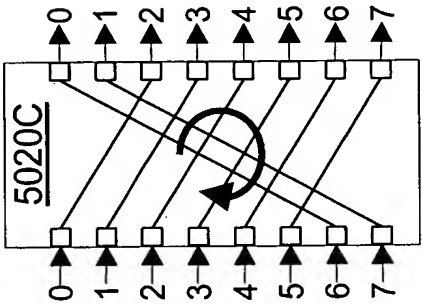
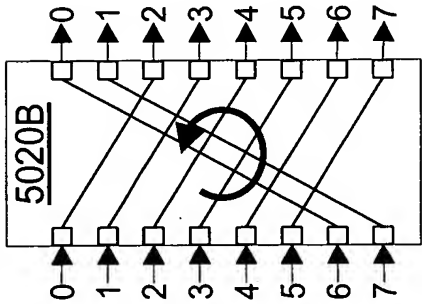
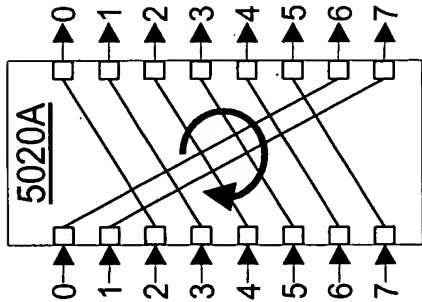


FIG. 52B

ROTATION PHASE  $t = 0$  ( $T=7$ )

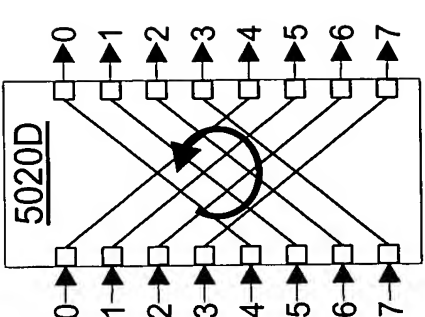
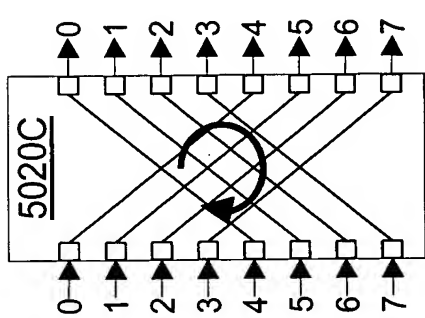
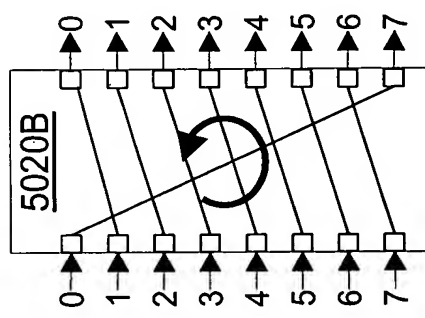
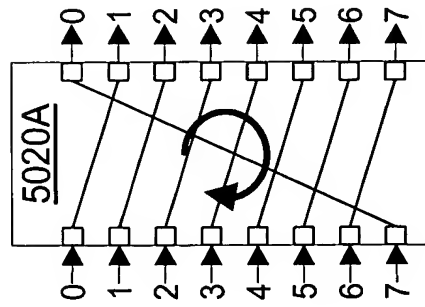


FIG. 53A

ROTATION PHASE  $t = 6$  ( $T=7$ )

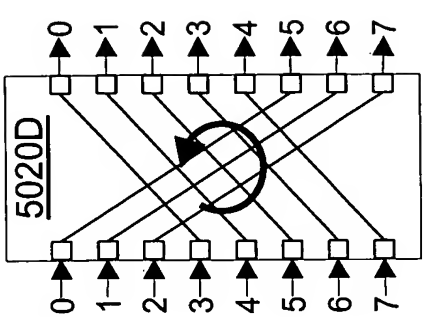
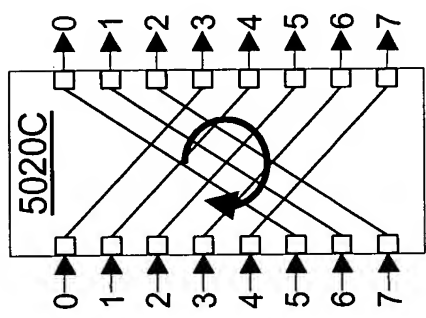
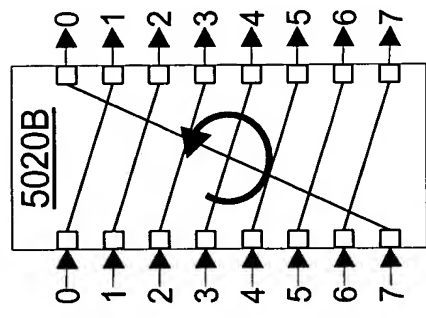
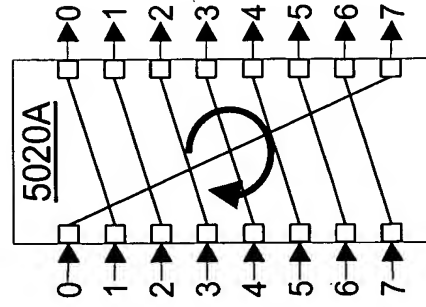


FIG. 53B

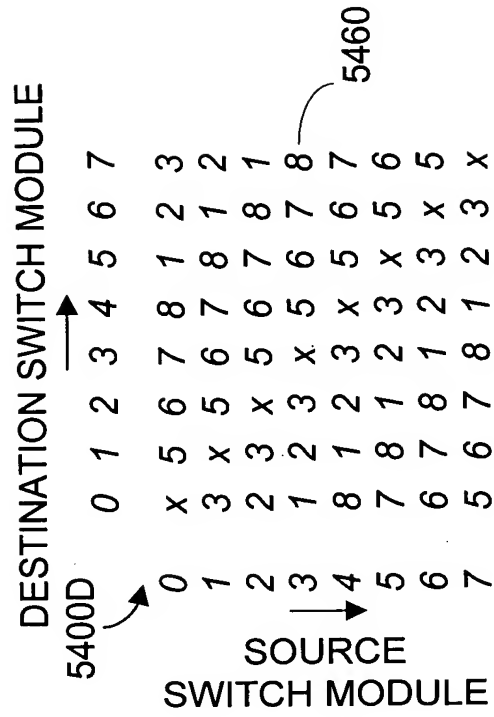
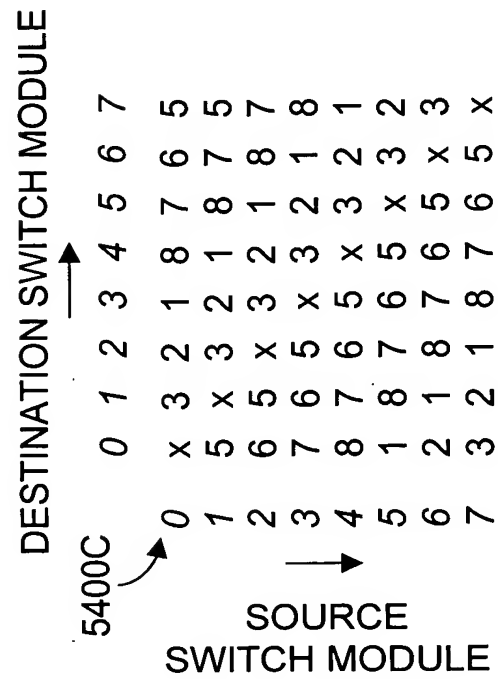
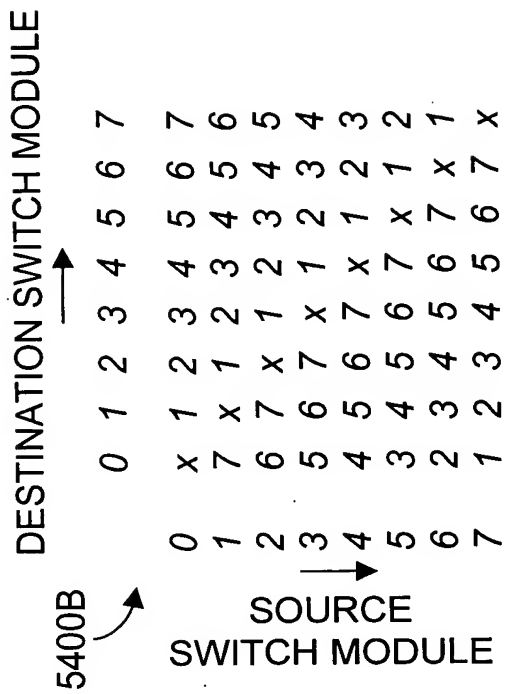
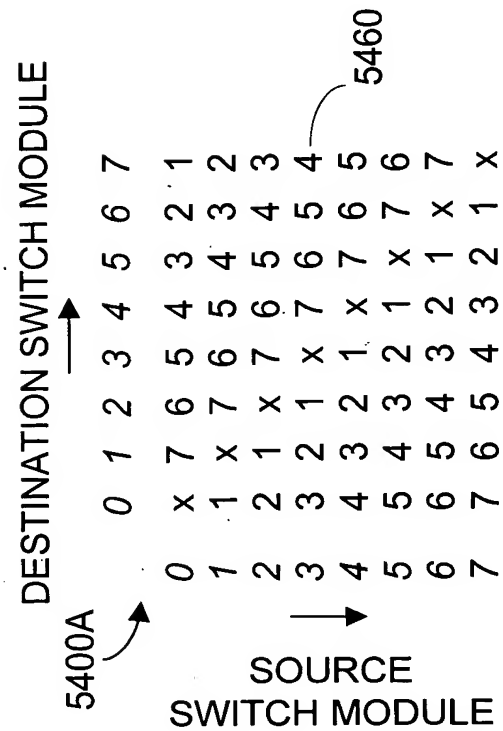
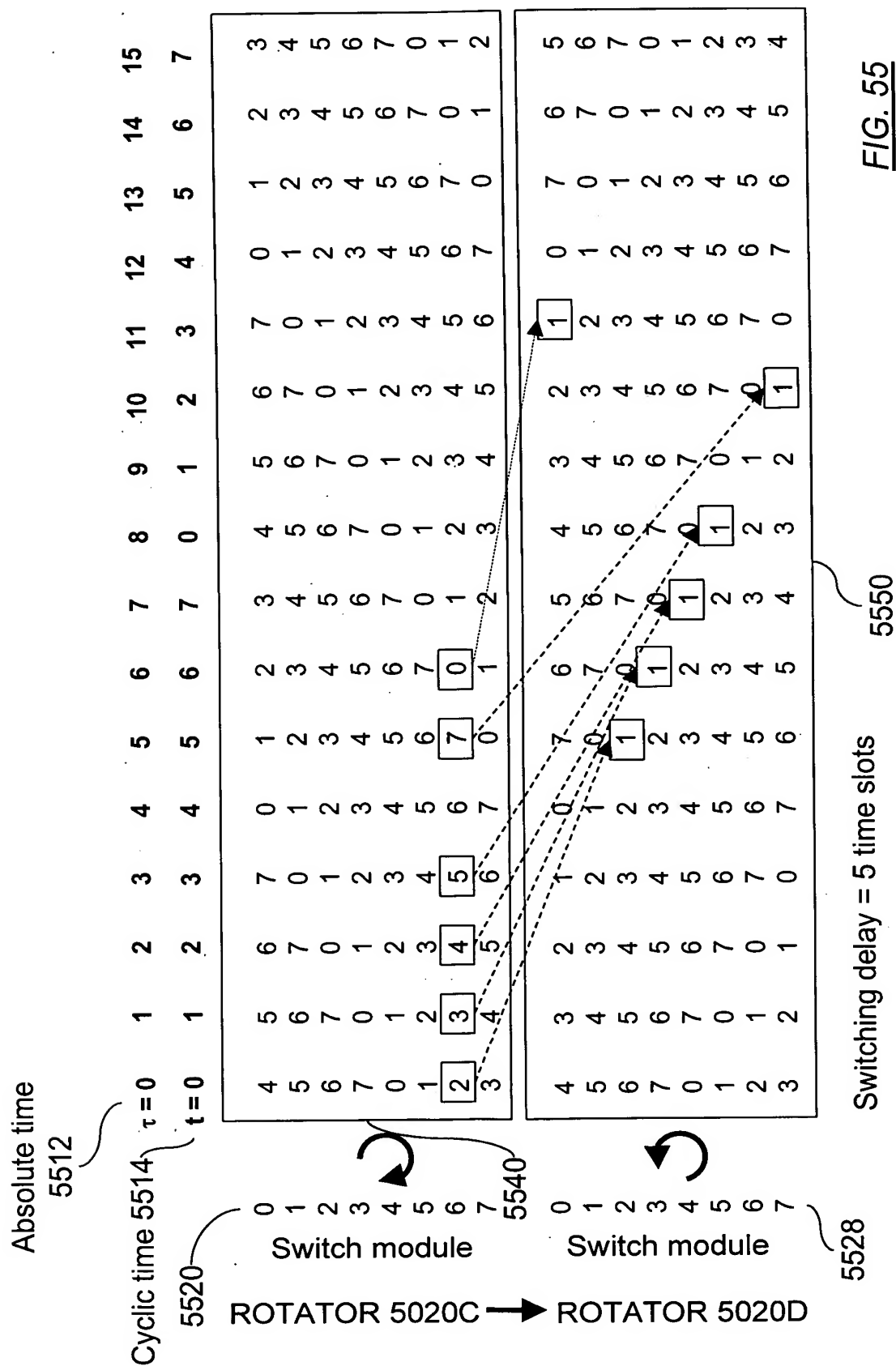


FIG. 54



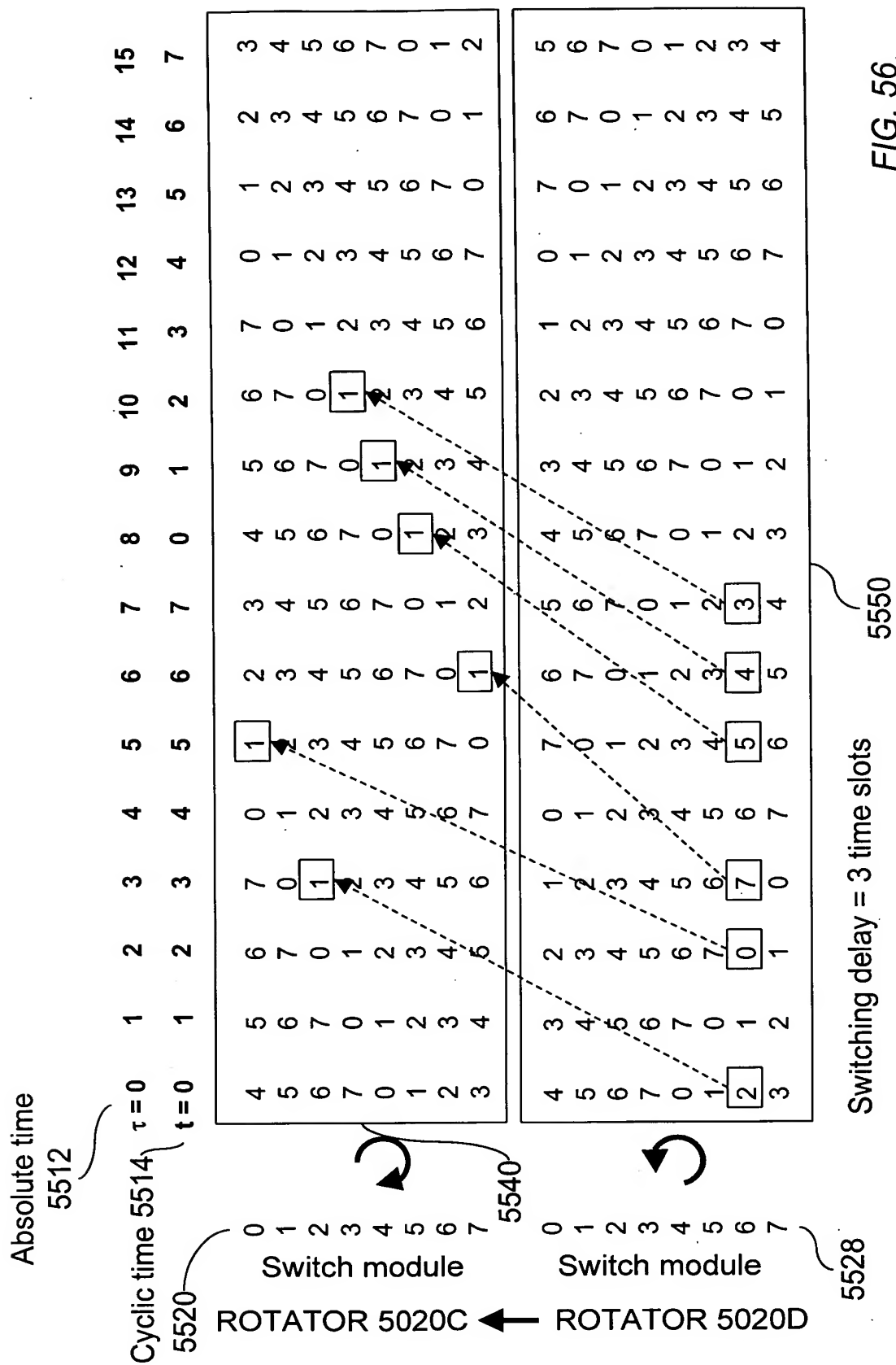


FIG. 56.



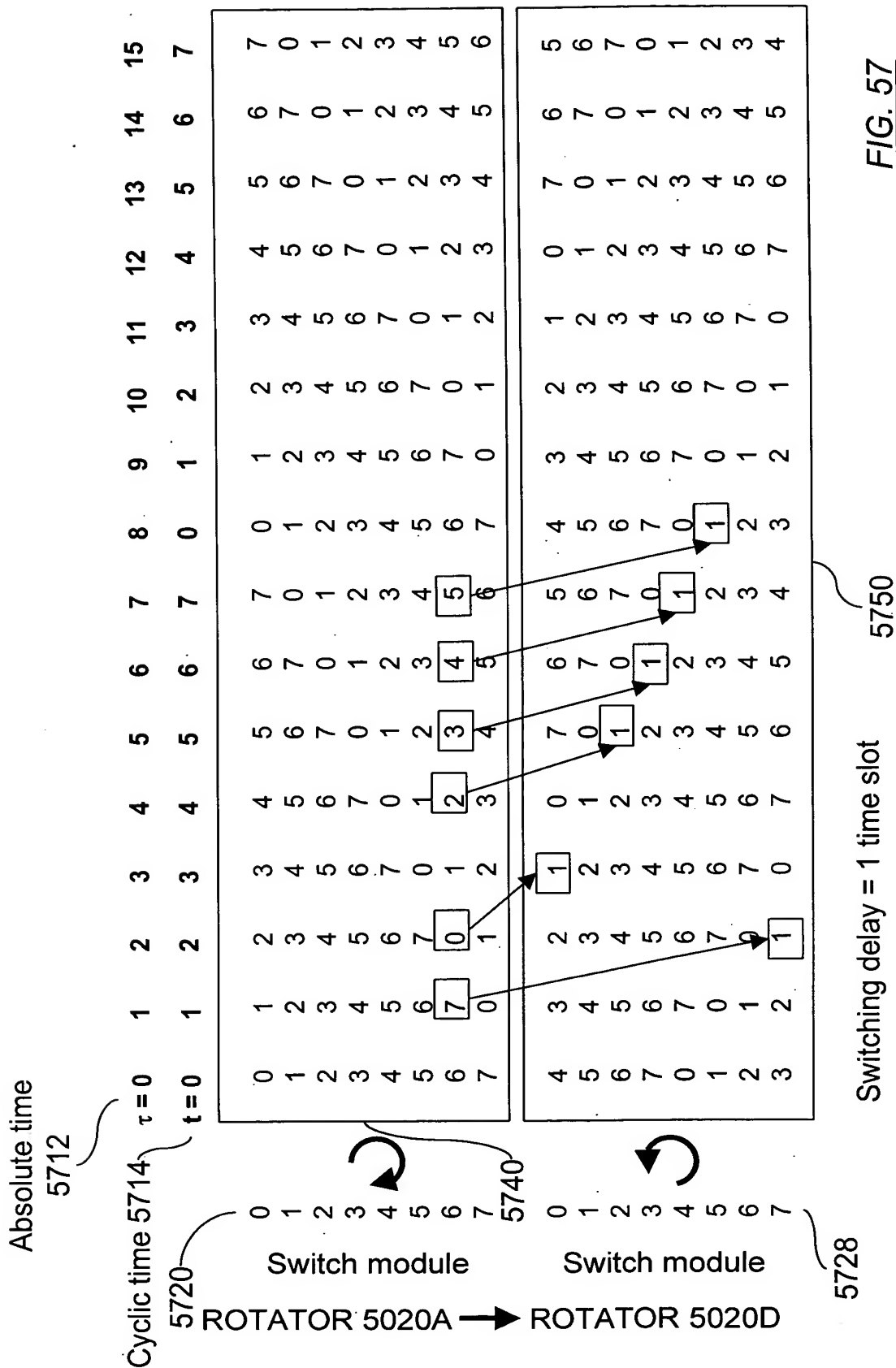


FIG. 57

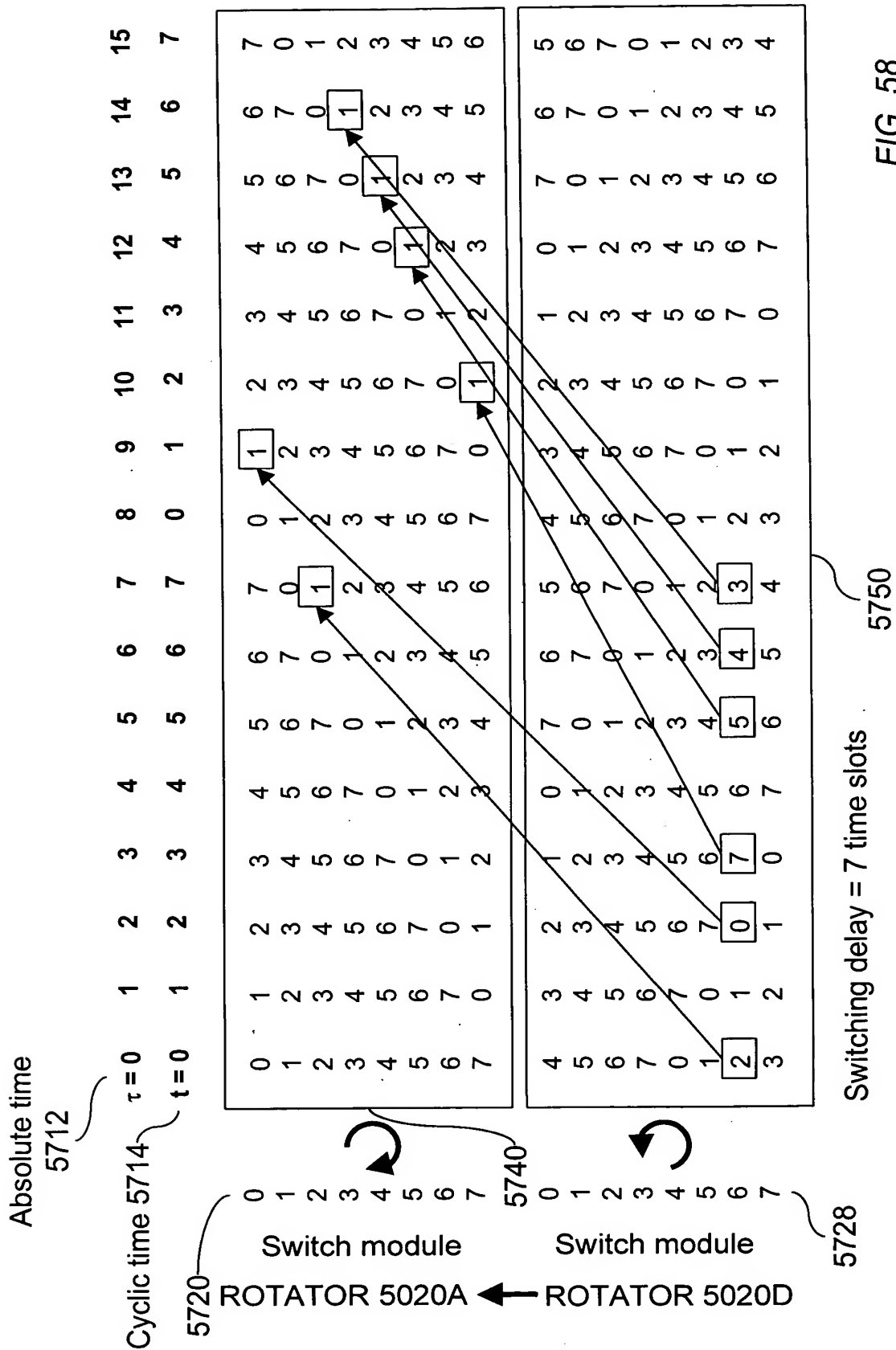


FIG. 58

Absolute time  
5912

Cyclic time 5914

$\tau = 0$   
 $t = 0$

5920

ROTATOR 5020C

5940

ROTATOR 5020B

5928

Switching delay = 1 time slot

5950

		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
Switch module	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2
	1	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
	2	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4
	3	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5
	4	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6
	5	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
	6	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0
	7	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1
Switch module	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6
	1	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
	2	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0
	3	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1
	4	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2
	5	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
	6	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4
	7	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5

FIG. 59

Absolute time  
5912

Cyclic time 5914  $\tau=0$

5920

Switch module

5940

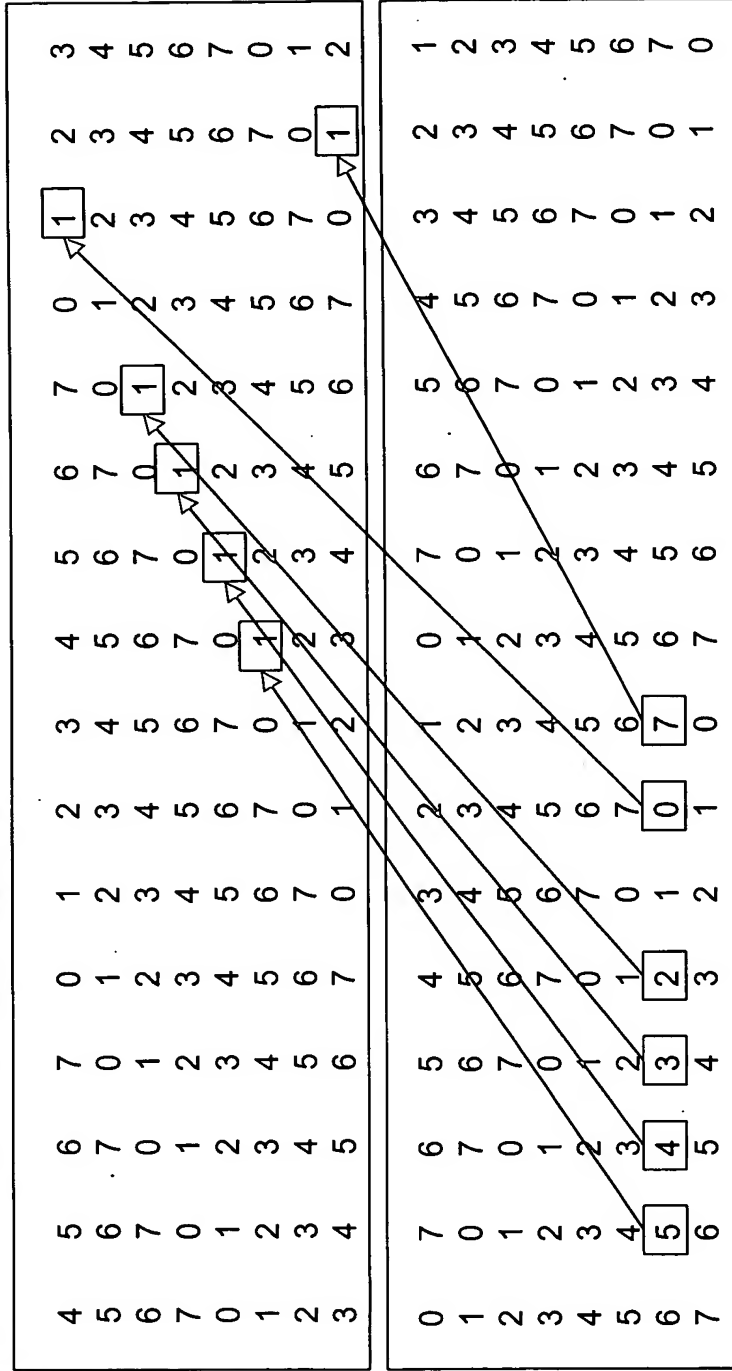
Switch module

5928

ROTATOR 5020C

ROTATOR 5020B

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15  
1 2 3 4 5 6 7 0 1 2 3 4 5 6 7



Switching delay = 7 time slots

5950

FIG. 60

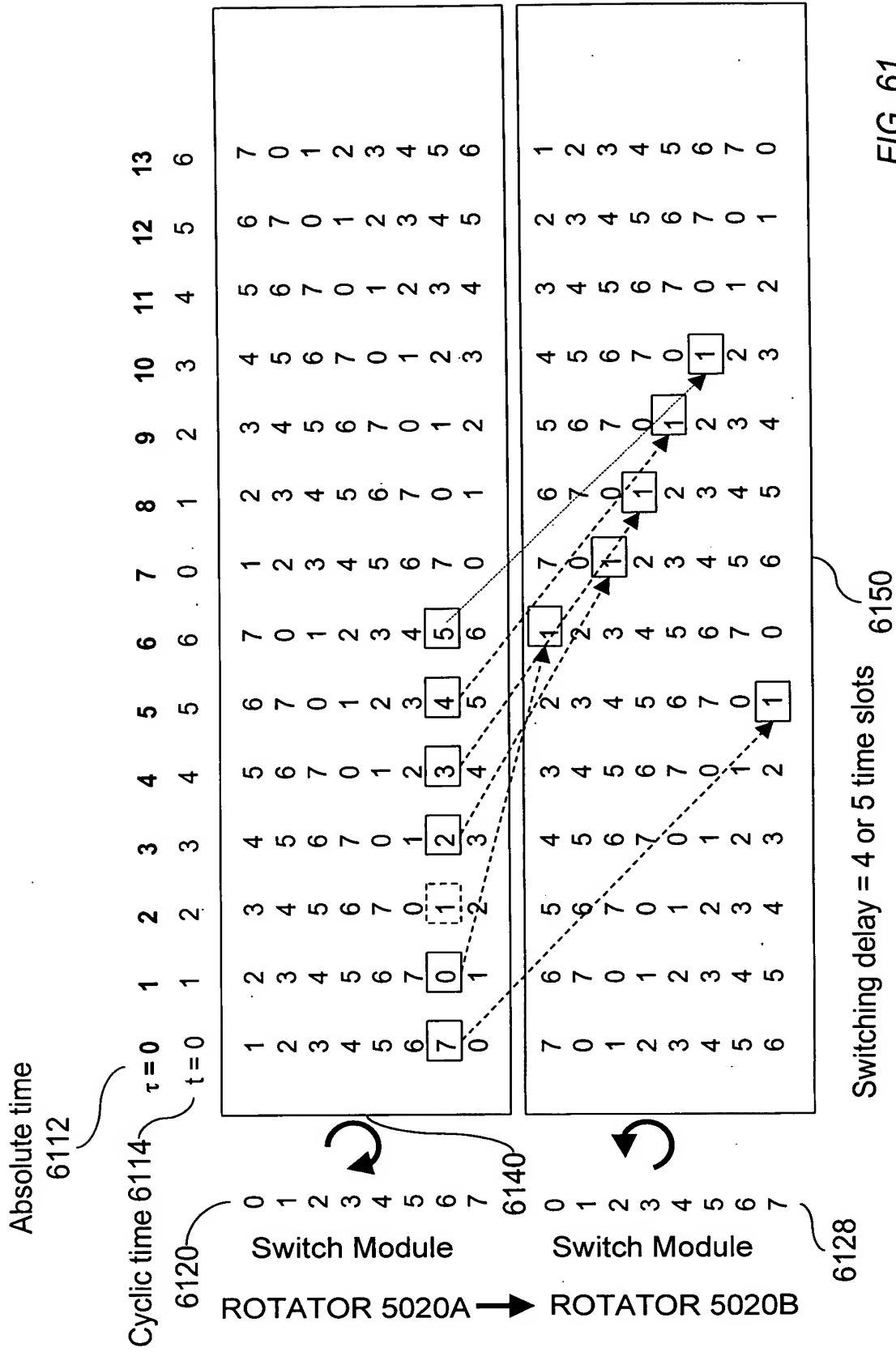


FIG. 61

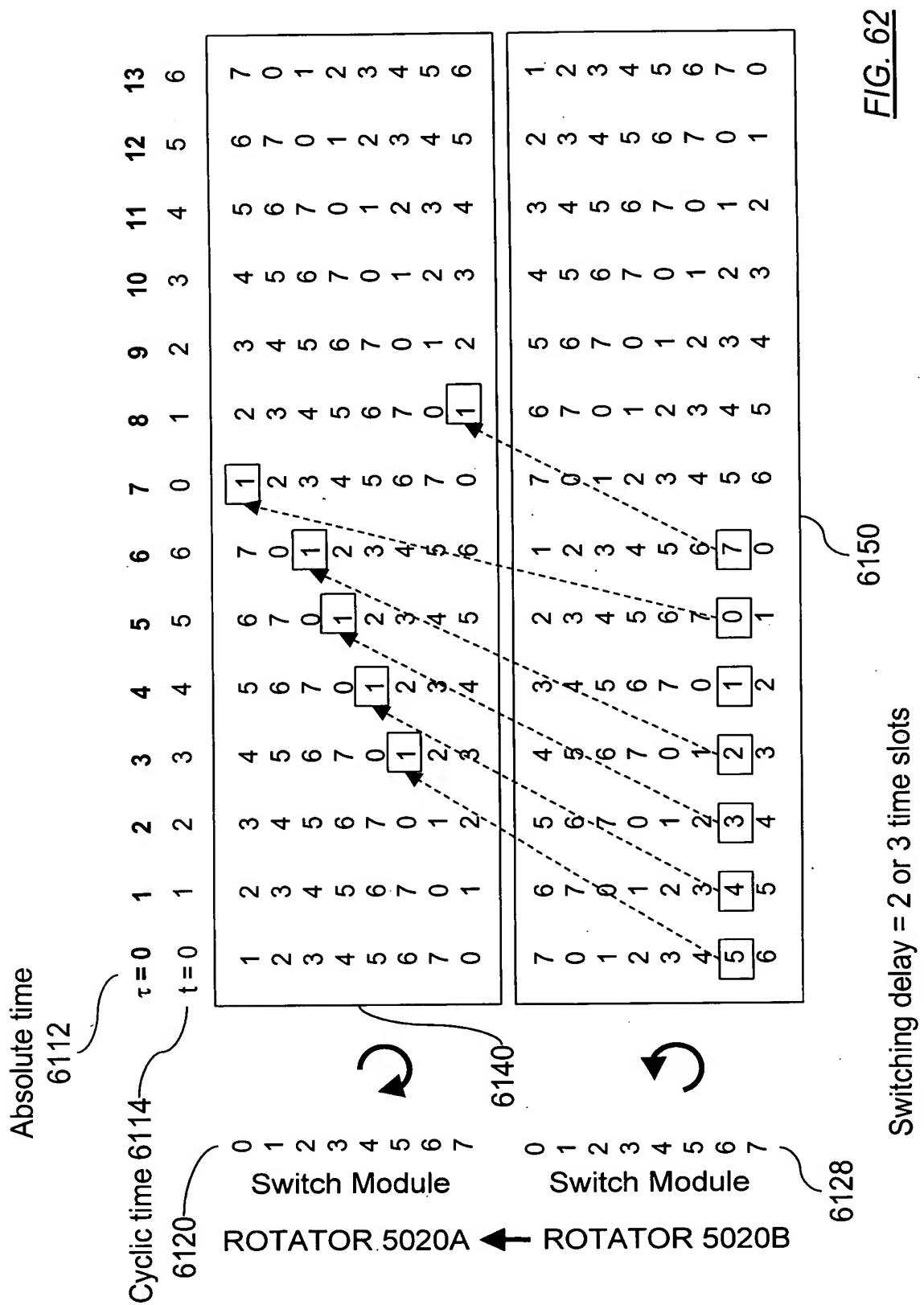
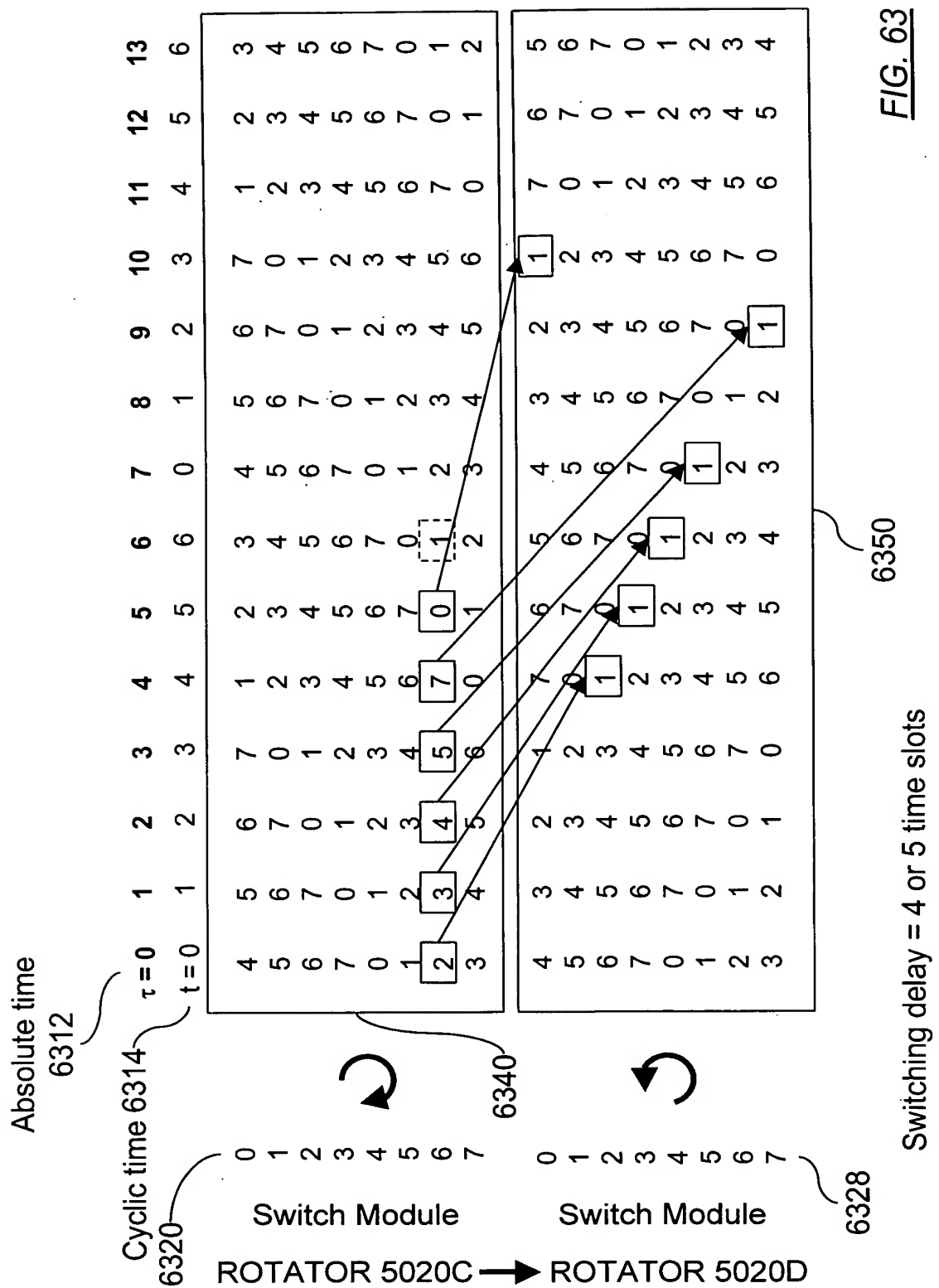
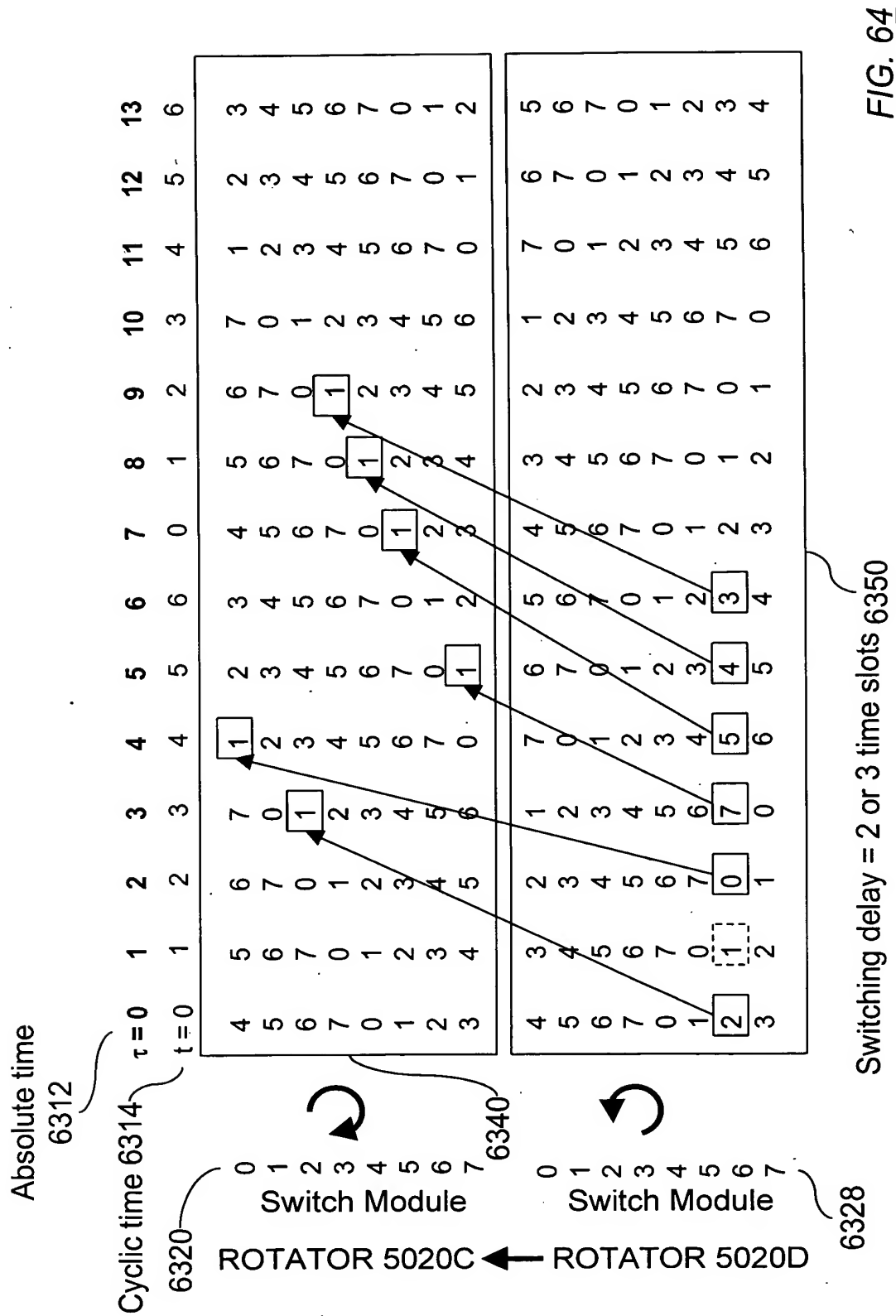


FIG. 62







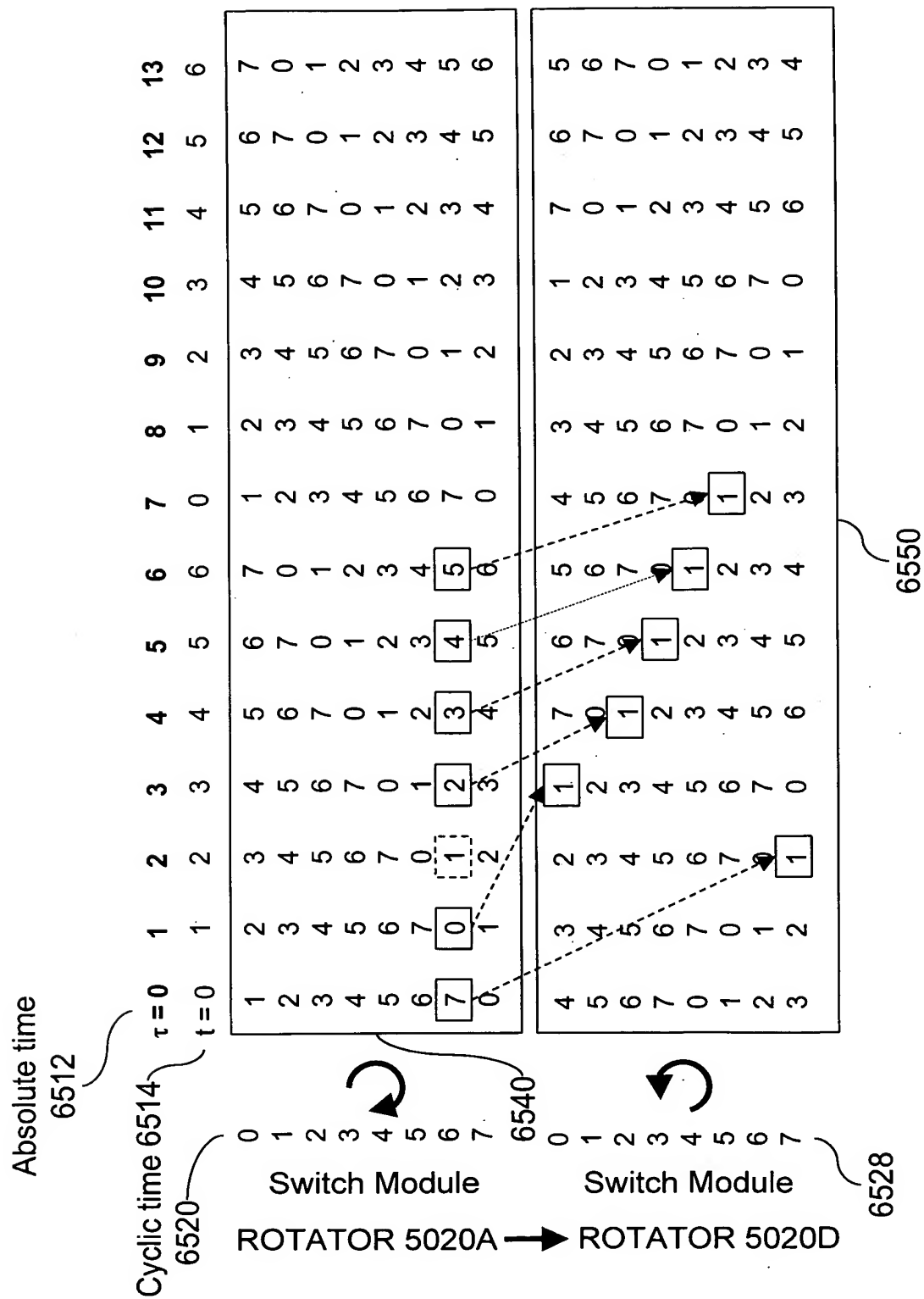


FIG. 65

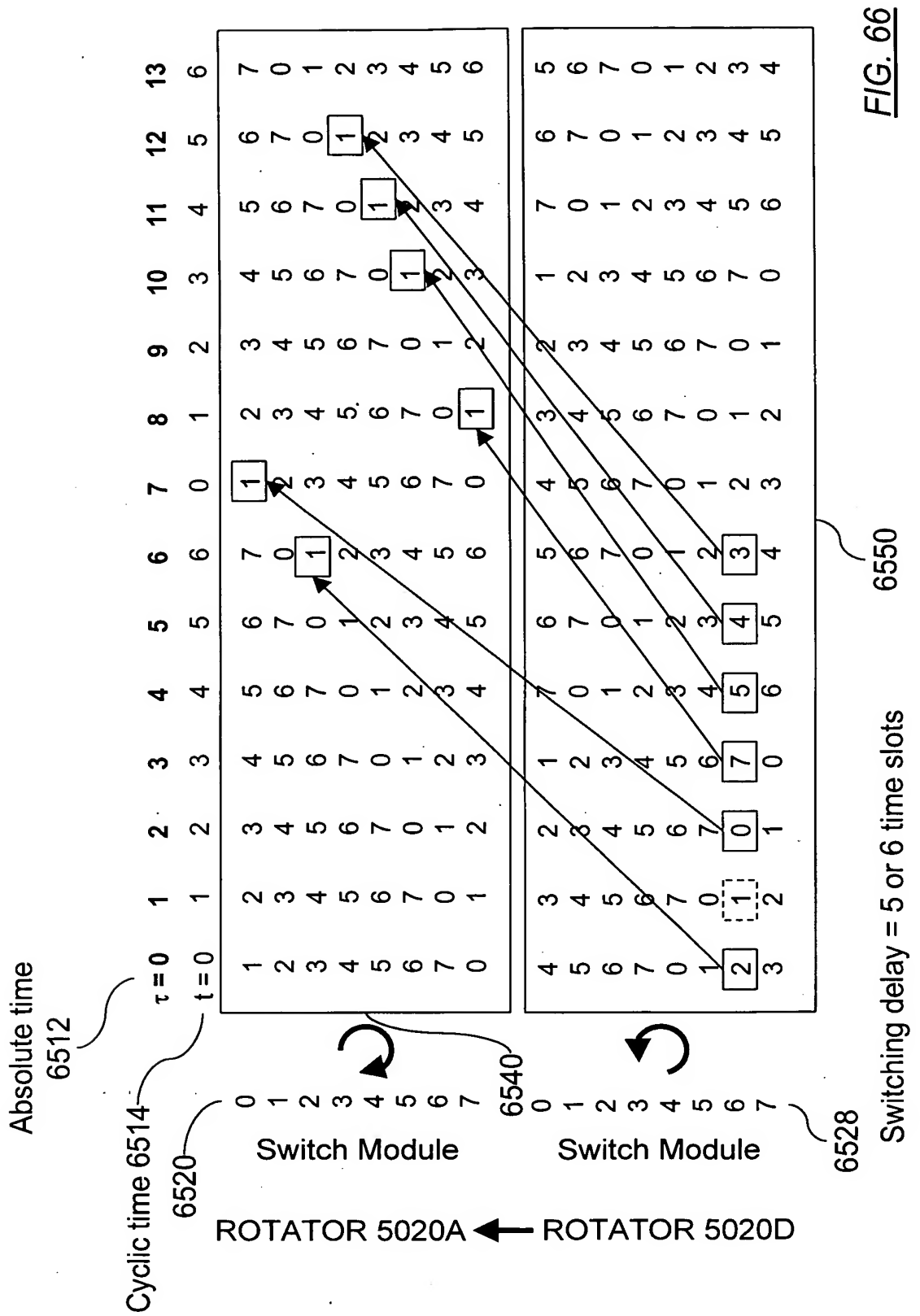


FIG. 66

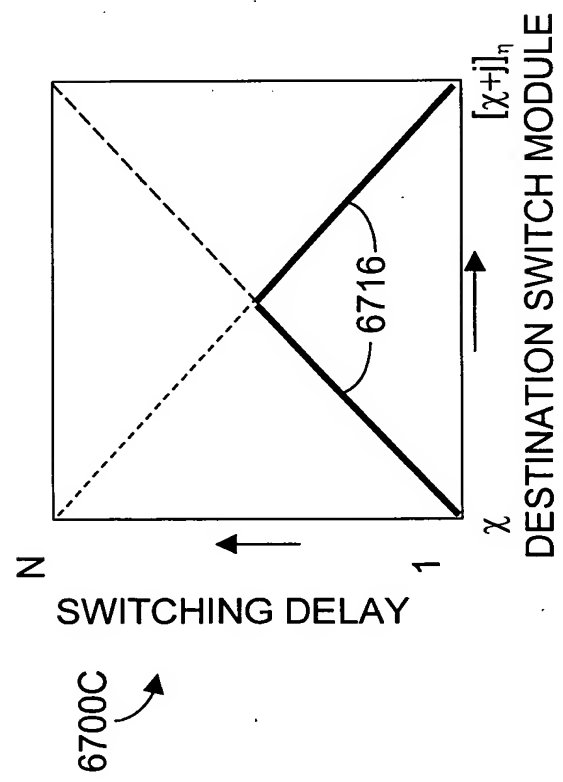
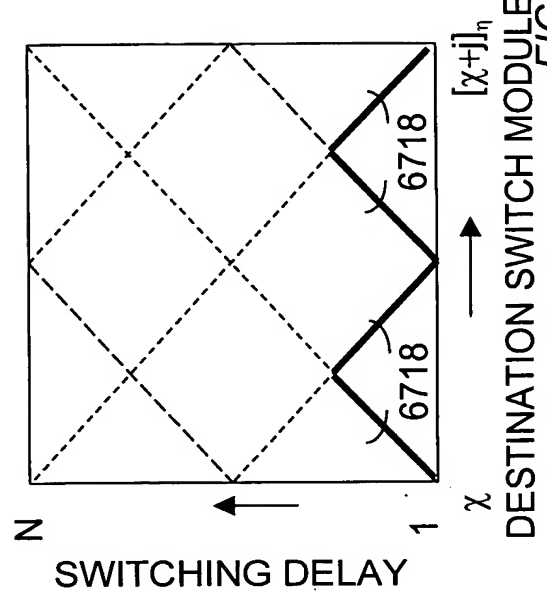
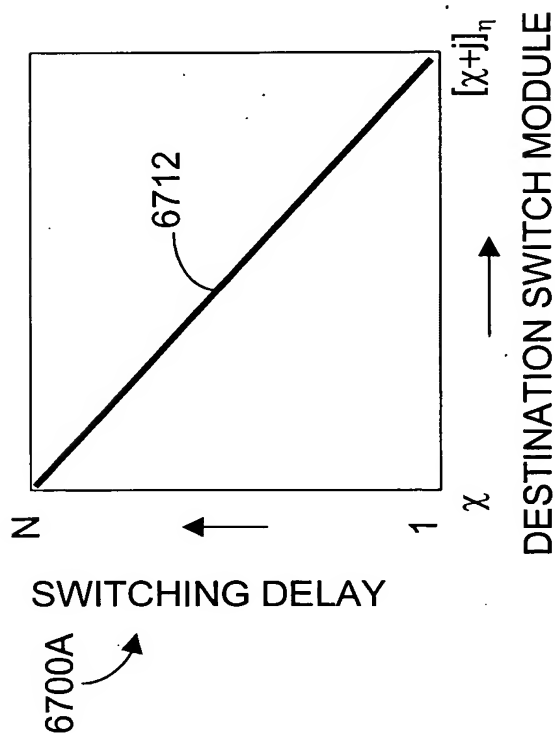
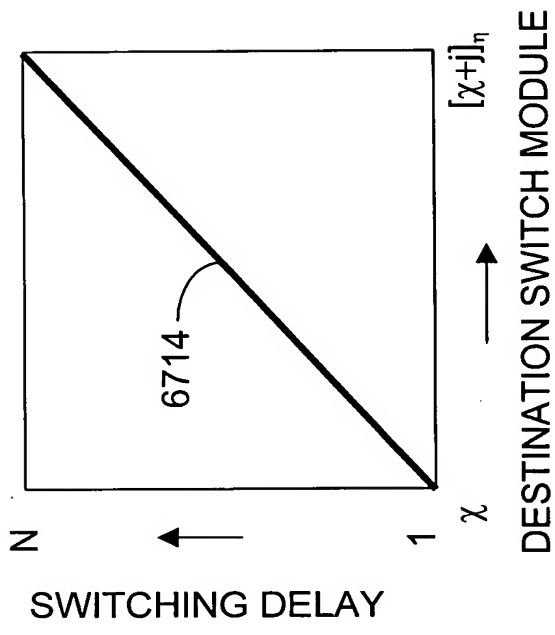


FIG. 67

		6824							6800						
		To switch module							DIRECT PATHS						
6823	From switch module	0	1	2	3	4	5	6	7						
		0	1	2	3	4	5	6	7						
	x	0 0	0 0	0 0	0 0	1 1	0 0	0 0	1 1						
	1 0	x	0 0	0 0	0 0	0 0	0 0	0 0	0 0						
	0 0	1 1	x	0 1	x	0 0	1 0	1 1	1 1						
	0 0	0 0	0 0	0 0	x	0 1	0 0	0 0	0 0						
	0 0	0 0	1 1	0 1	0 1	x	1 0	0 0	0 0						
	0 0	1 1	1 0	0 0	0 0	0 0	x	1 0	1 1						
	0 0	1 1	1 1	0 0	0 0	0 0	0 0	x	1 1						
	0 0	1 0	0 1	1 1	1 1	0 1	1 0	0 1	x						

FIG. 68

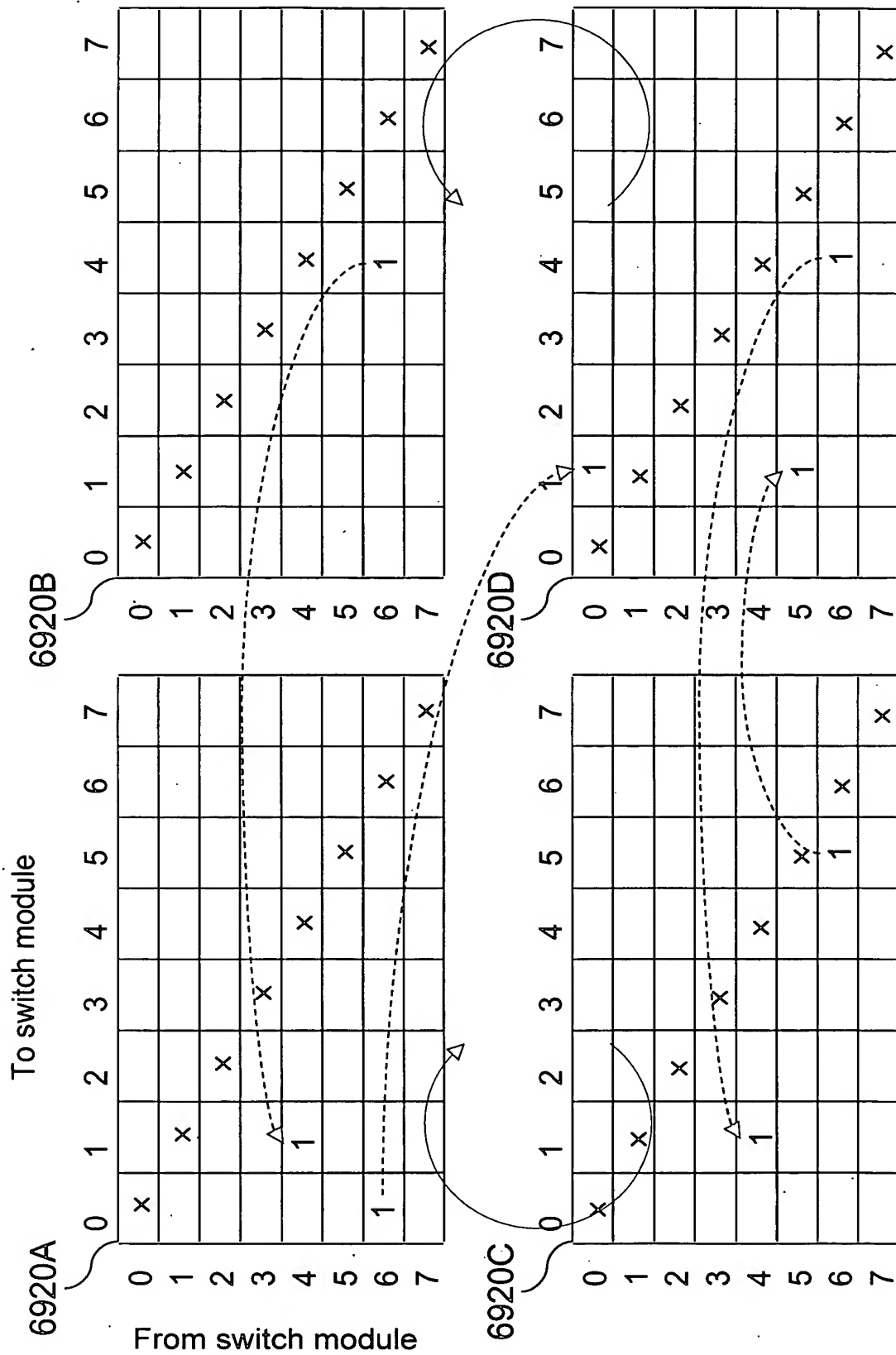


FIG. 69

		DIRECT PATHS								
		To switch module								
		0	1	2	3	4	5	6	7	
7000 ↗	7023 ↘	0	x	000 000	000 000	000 000	010 110	000 000	000 000	010 010
	1	110 000	x	000 000	000 000	000 000	000 000	000 000	000 000	000 000
	2	000 000	010 110	x	000 101	000 000	000 000	110 000	110 010	010 110
	3	000 000	000 000	000 000	x	000 101	000 000	000 000	000 000	000 000
	4	000 000	000 000	010 110	000 110	x	010 000	000 000	000 000	000 000
	5	000 000	010 110	110 000	000 000	000 000	x	101 000	010 110	010 110
	6	000 000	110 001	010 110	000 000	000 000	000 000	x	010 110	010 110
	7	000 000	001 000	000 110	110 110	000 001	010 000	000 010	000 000	x

FIG. 70

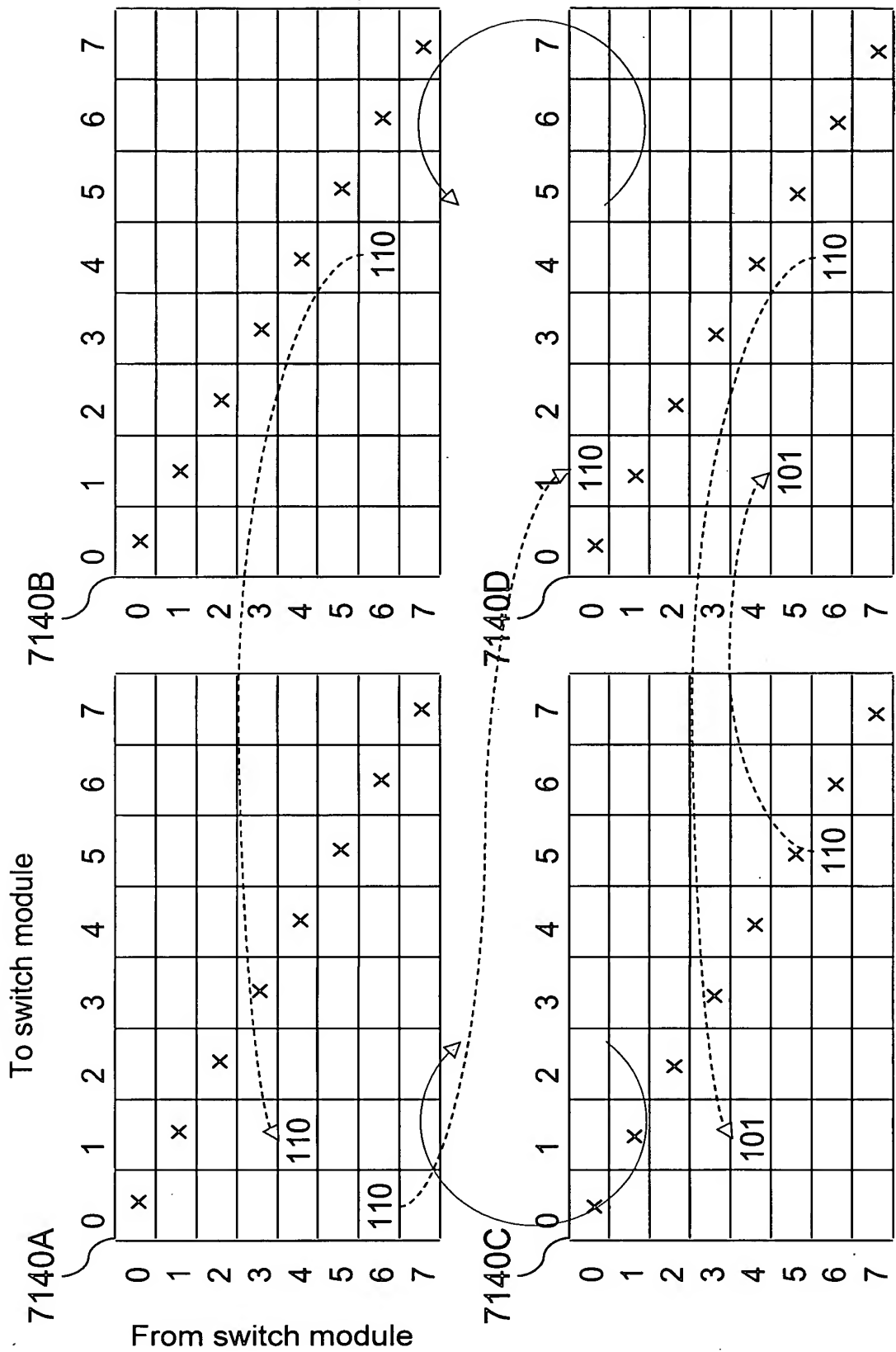
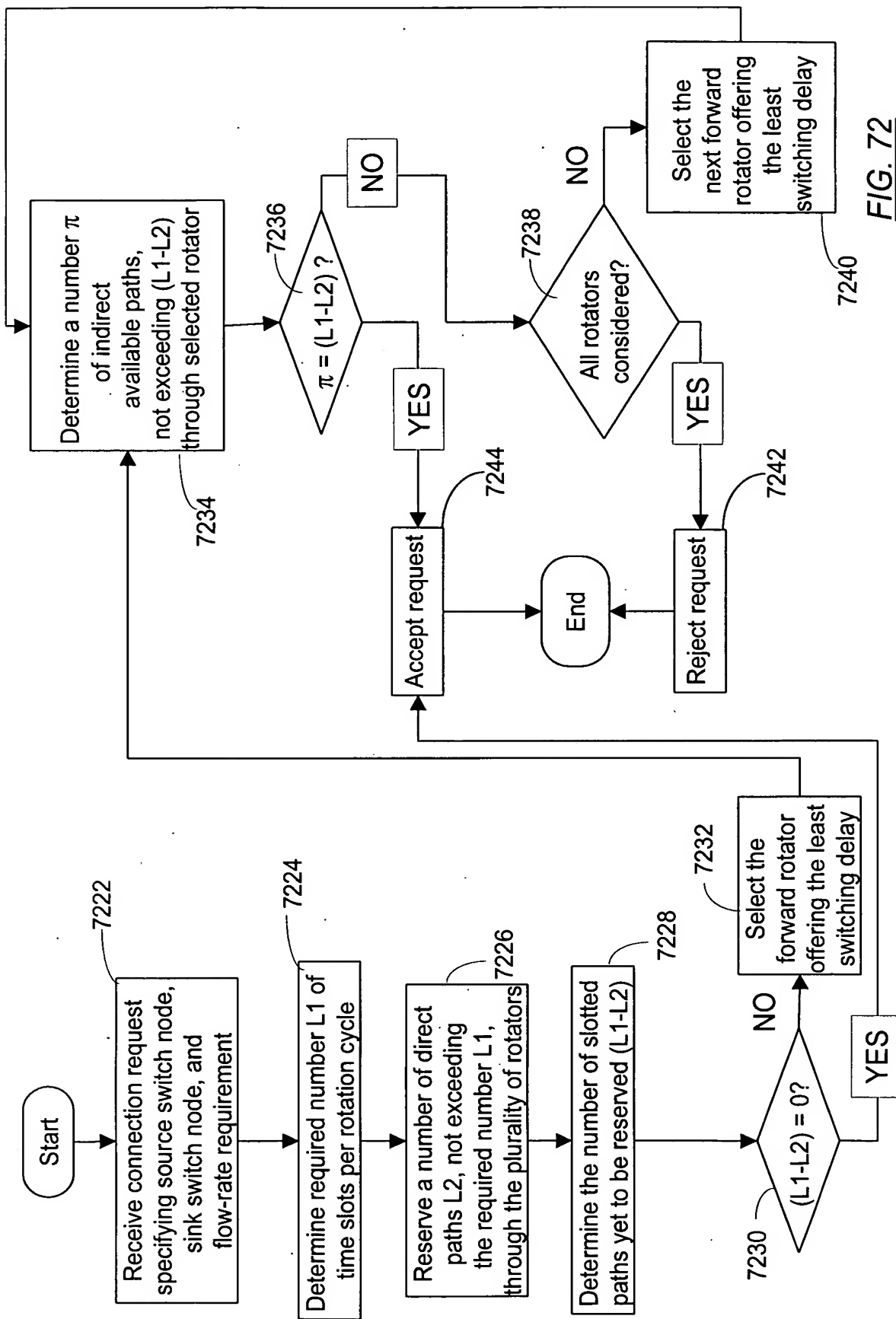


FIG. 71





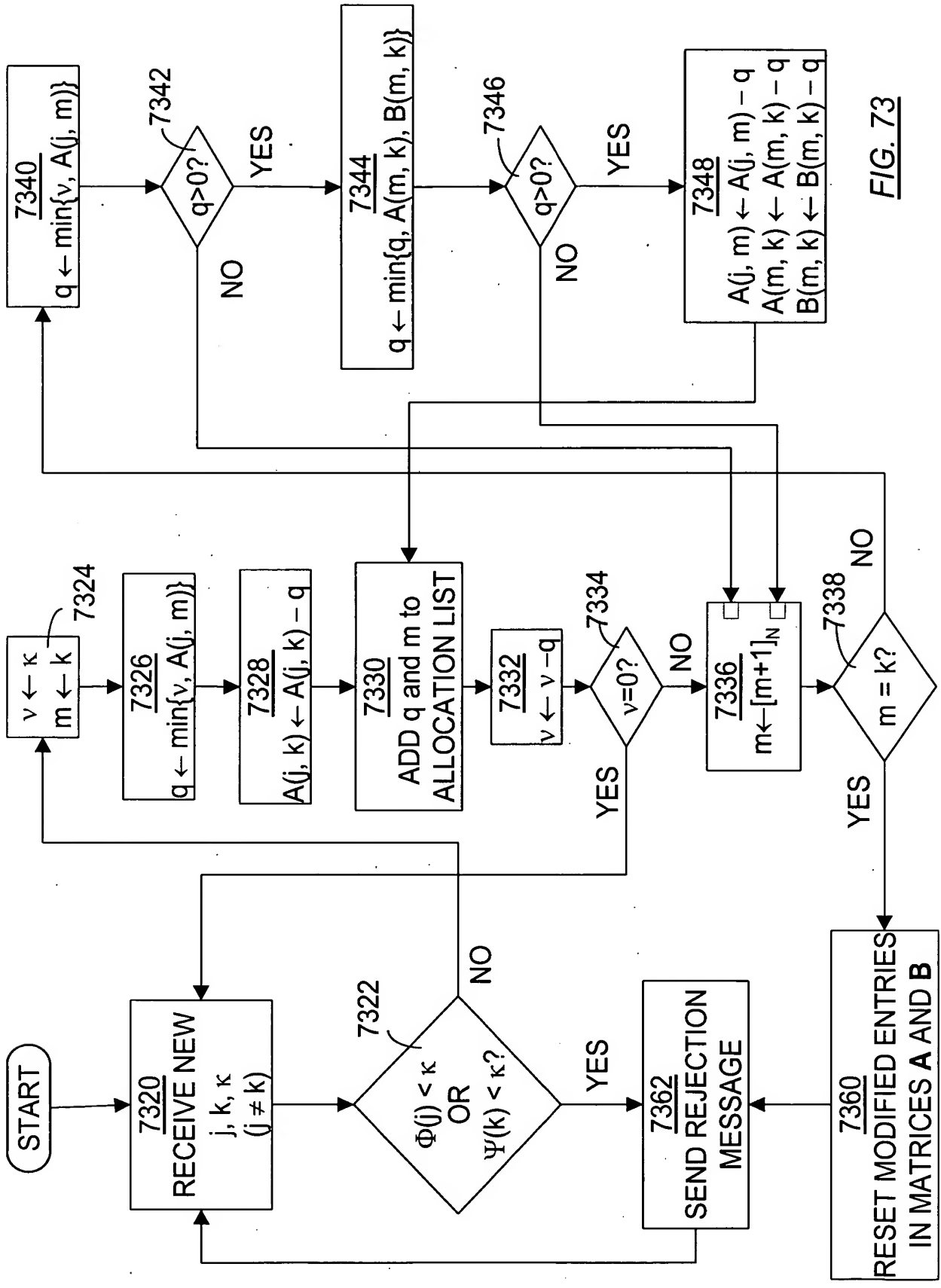


FIG. 73

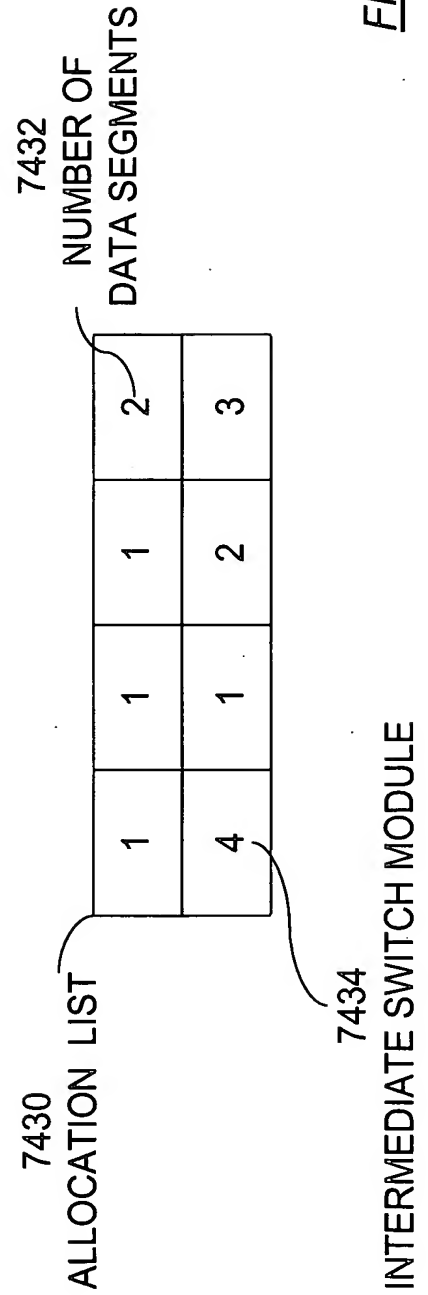
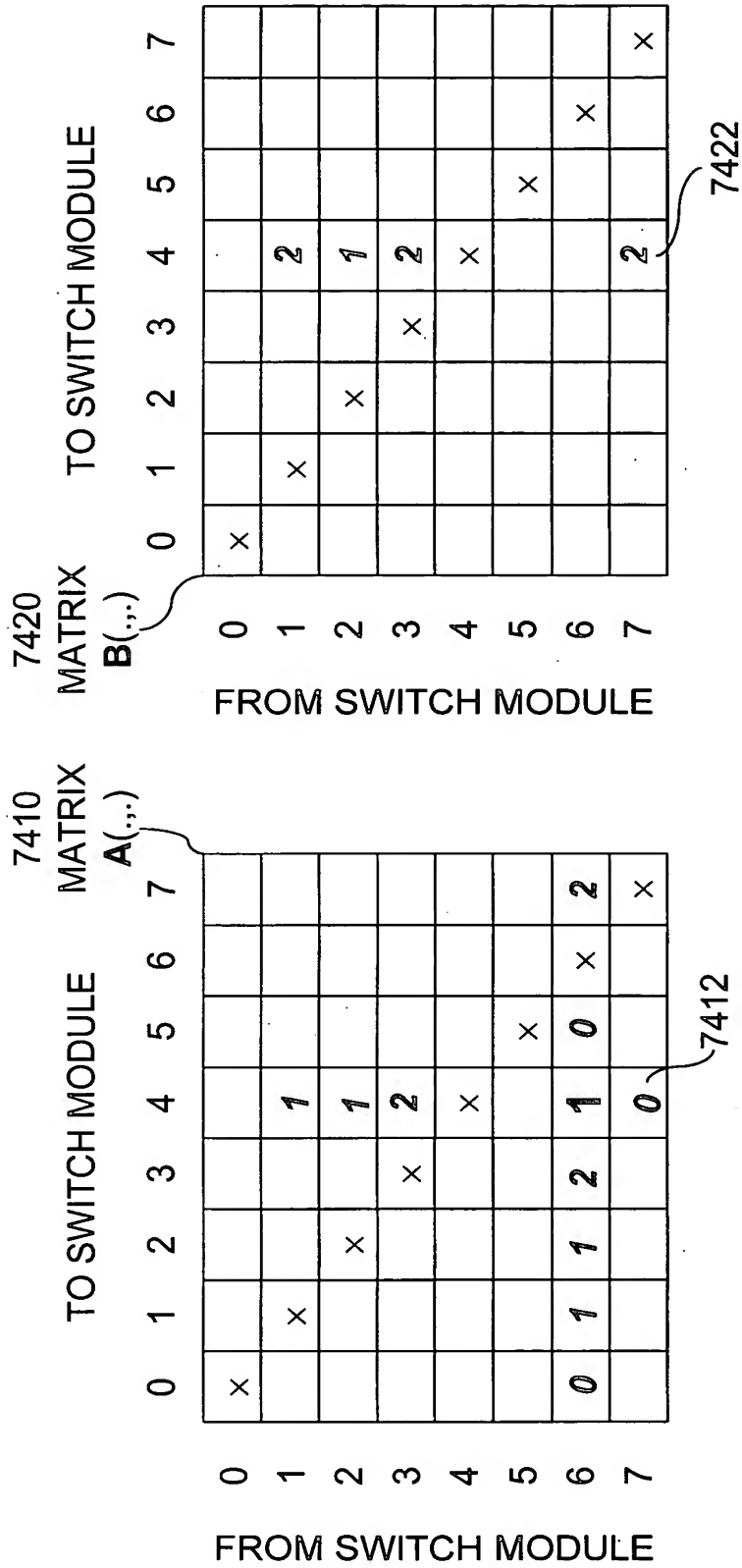
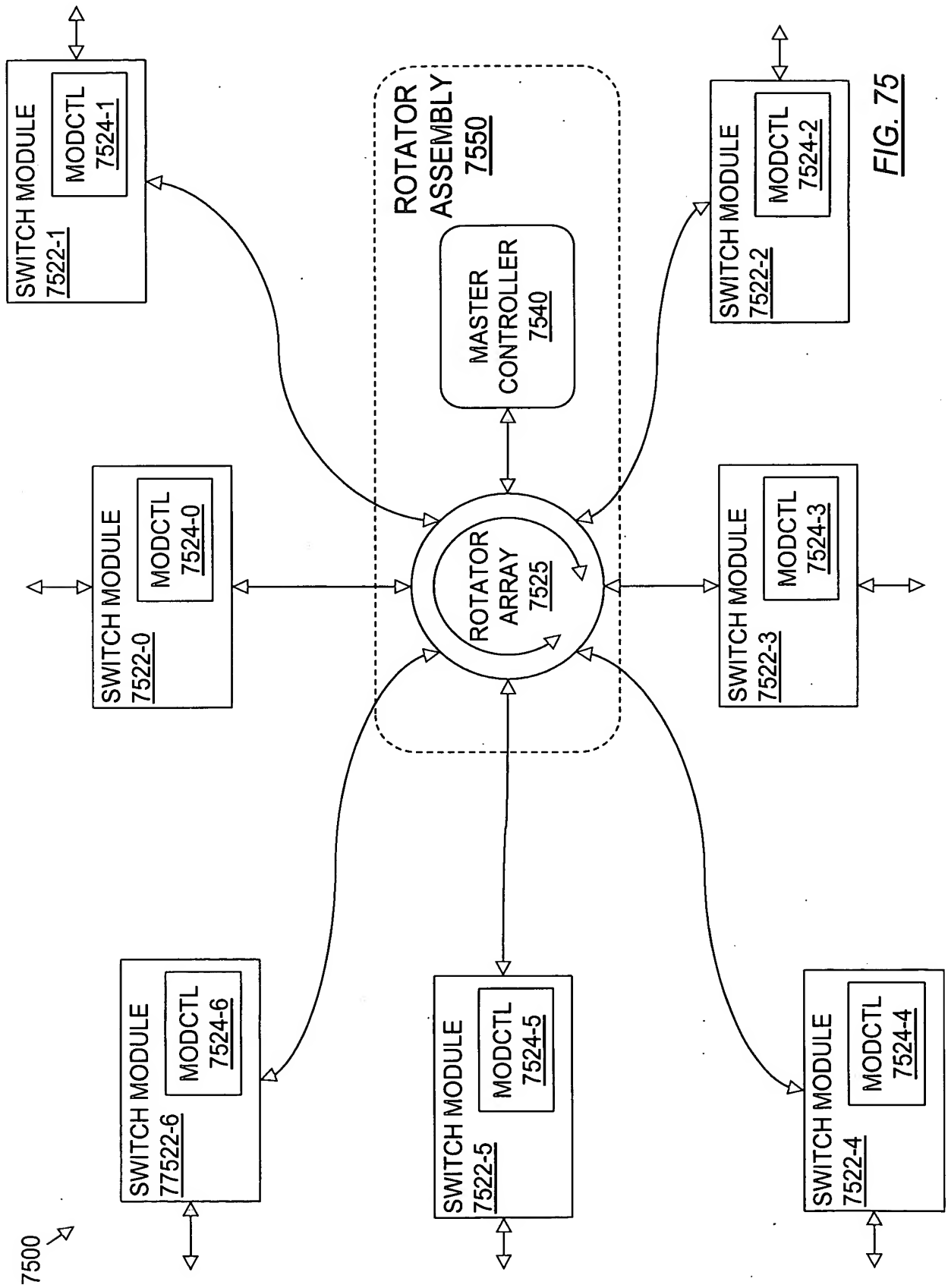


FIG. 74



**FIG. 75**

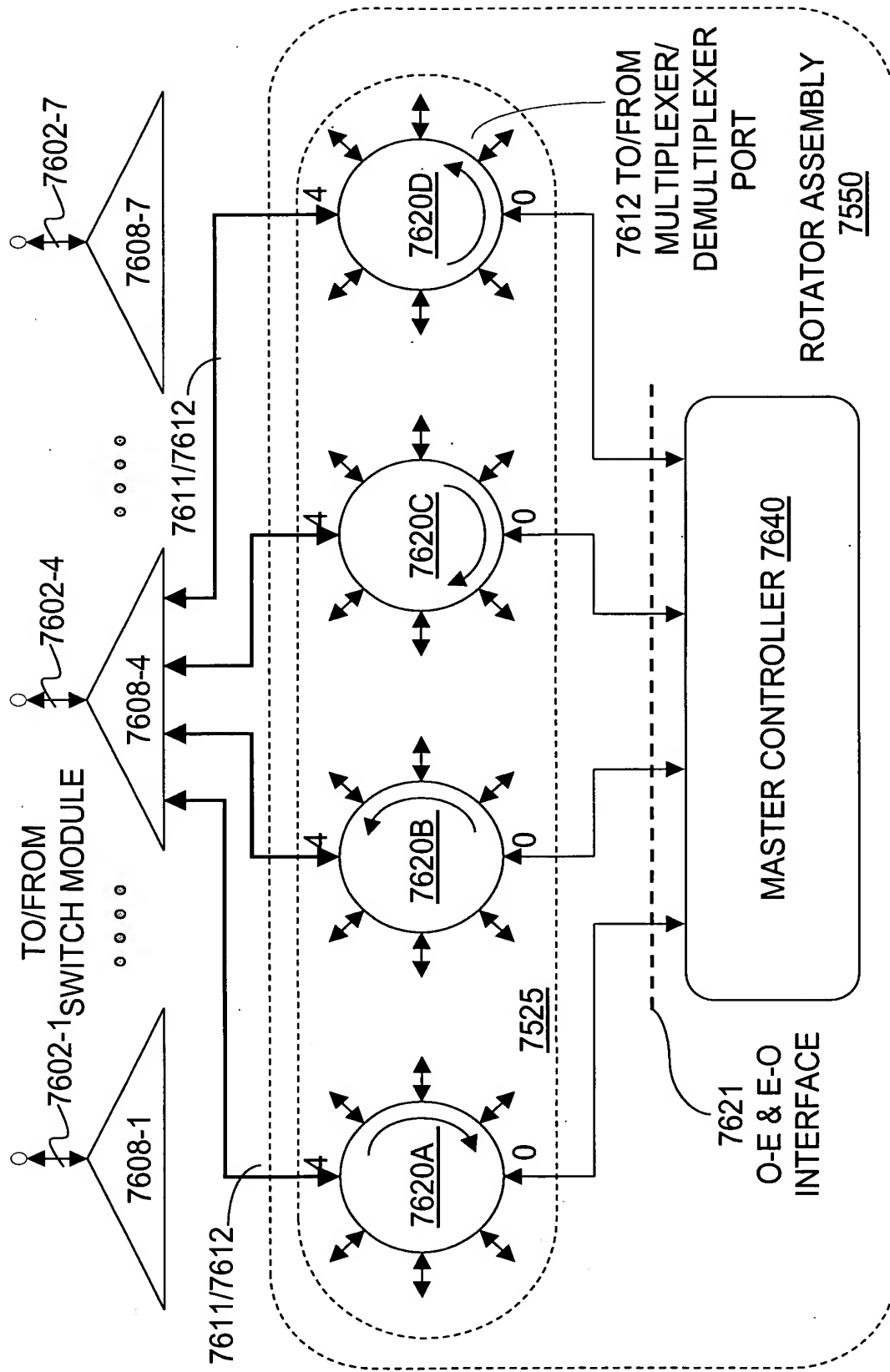


FIG. 76

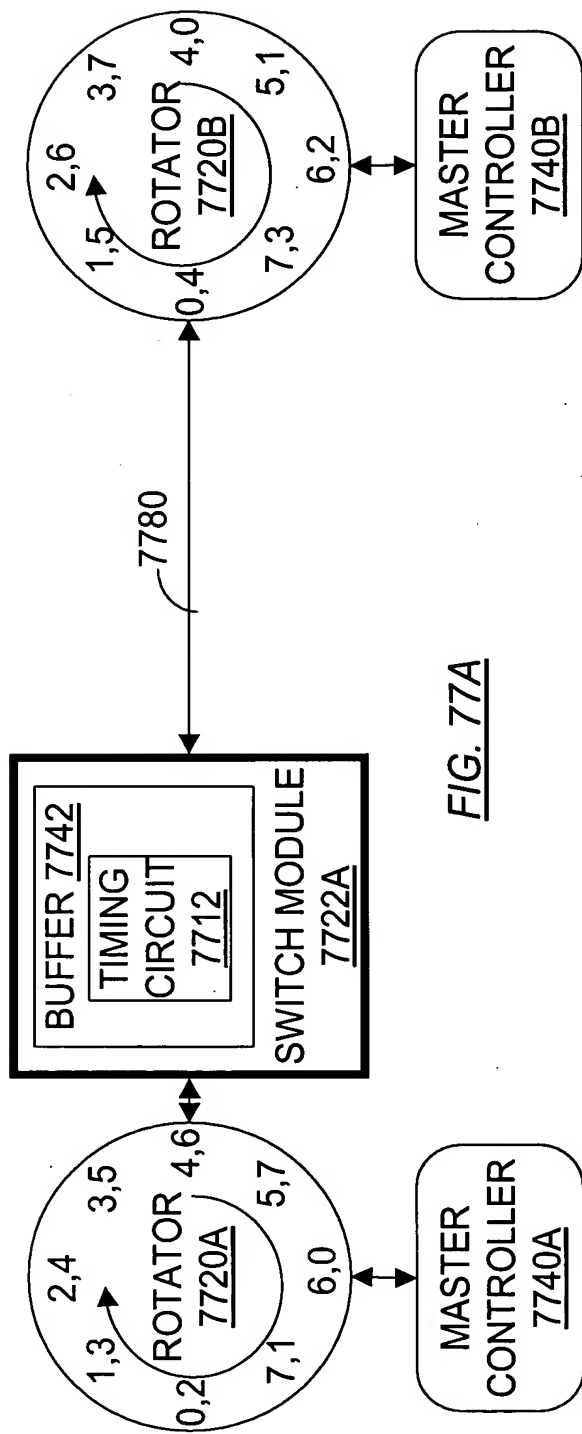


FIG. 77A

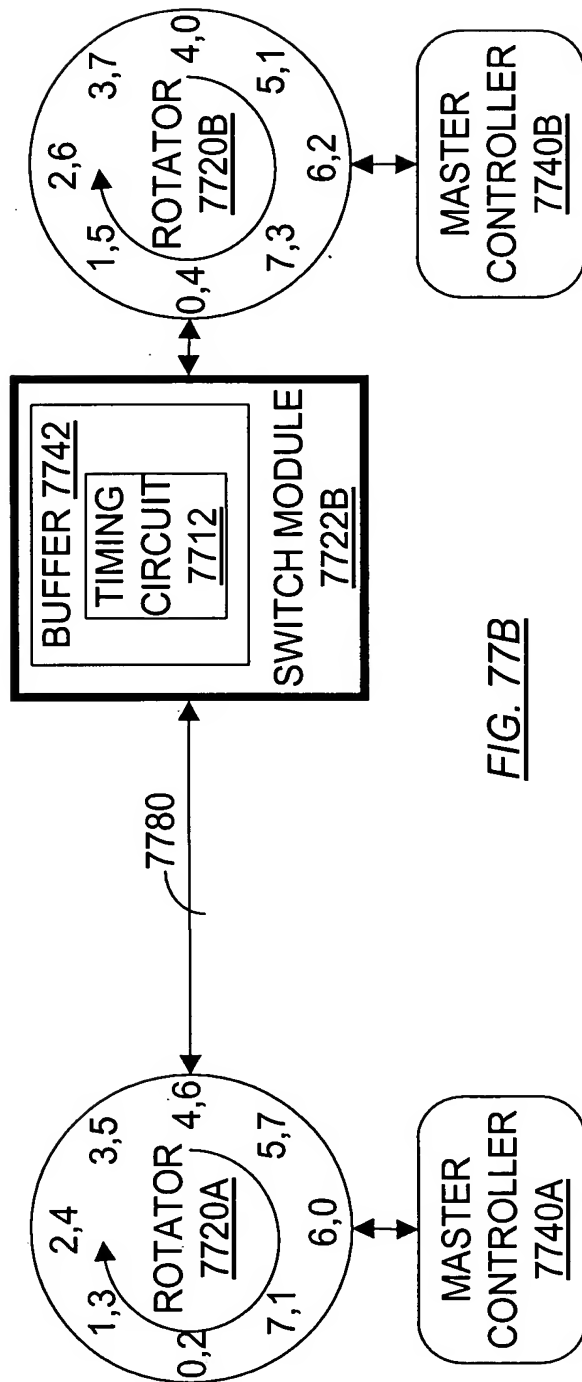


FIG. 77B

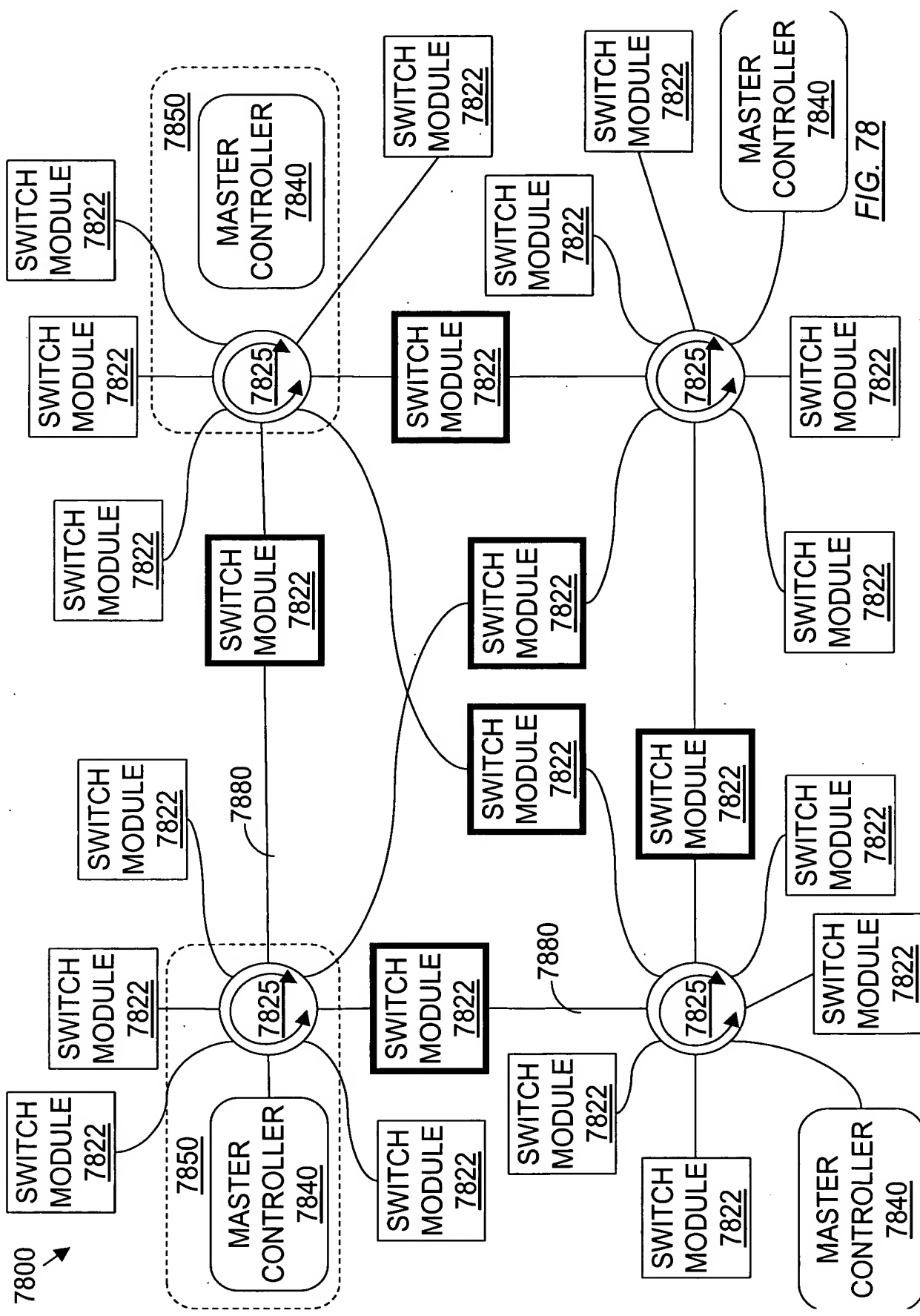


FIG. 78

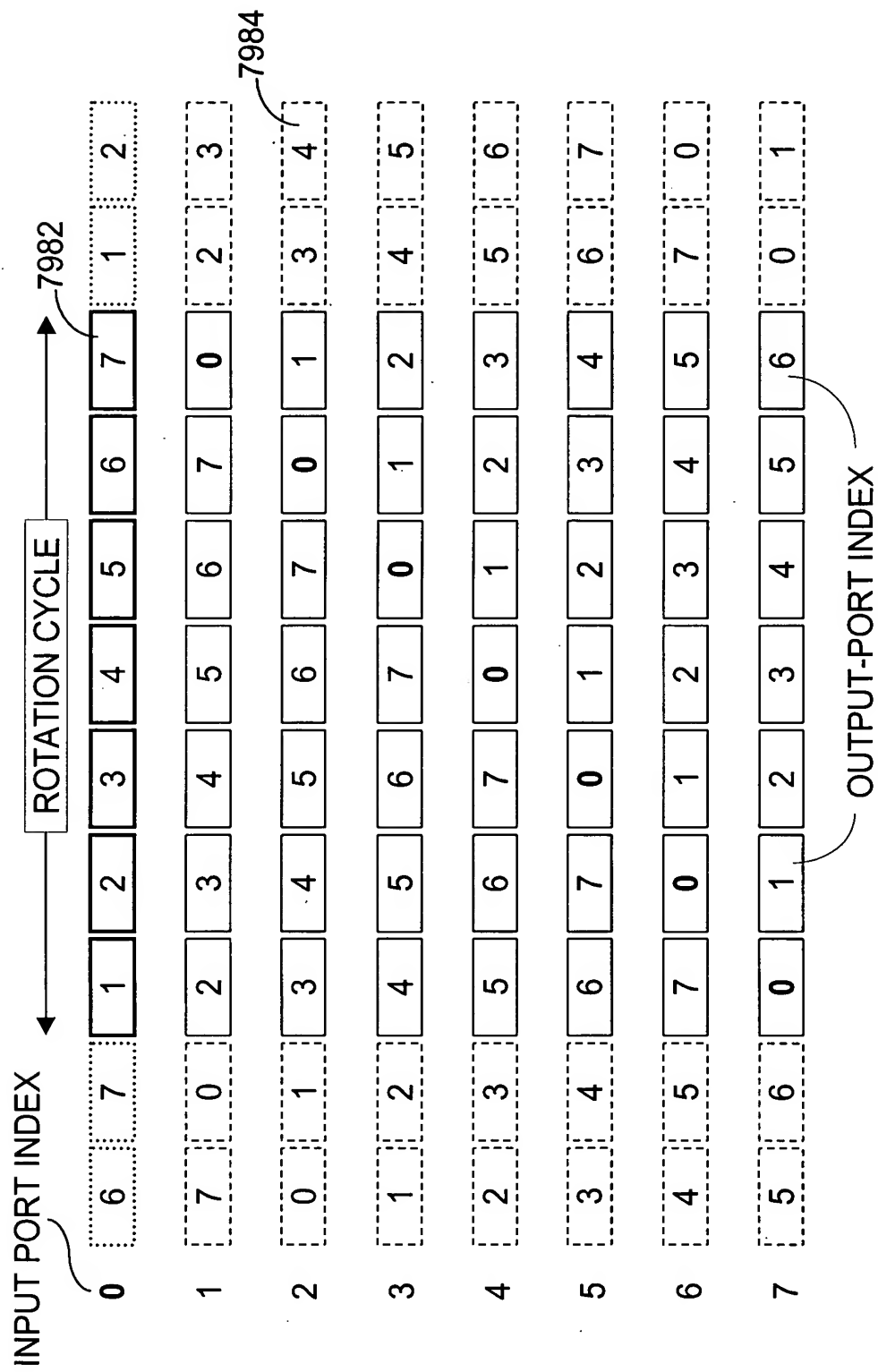


FIG. 79

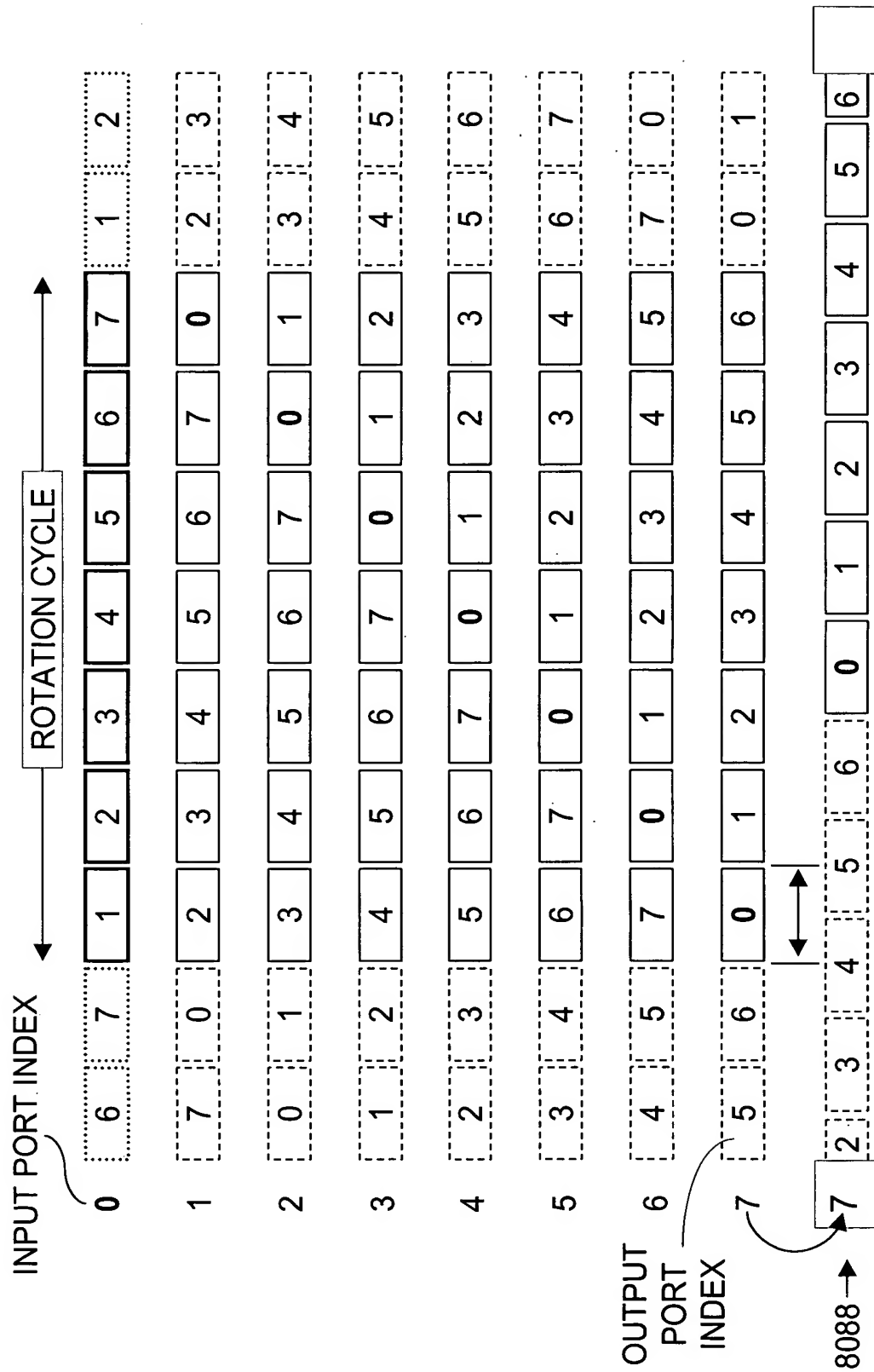


FIG. 80